

# Extended Range Second Order Digital Phase Locked Loop

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**Abstract**—Phase error dynamics of a conventional second order Digital Phase Locked Loop (DPLL) and that of a newly proposed modified second order DPLL (MSODPLL) have been studied using digital computers. Ranges of initial conditions leading to the phase locking condition were determined from computer simulation of both conventional and modified second order DPLL. Lyapunov exponents were also examined, for very large number of possible values of the state variables (phase errors) with same input conditions in both the loops. Using these observations the superiority of the MSODPLL for the frequency acquisition range over conventional DPLL has been established.

**Index Terms** --Digital PLL, DPLL phase error dynamics, Chaos in DPLL

## I. INTRODUCTION

Nonuniforms sampling digital Phase Locked Loops (DPLLs) are widely used in coherent communication system. DPLLs are replacing its analogue counterpart as it minimize some of the problems associated with the loops such as sensitivity to DC drift and the need for periodic adjustments etc. The most popularly used DPLL is the positive going zero-crossing sampling type digital phase-locked loop (ZC<sub>1</sub>-DPLL) [1]. This loop is popular among the user as it is easy to implement in hardware and simple to model mathematically. Application of second order ZC<sub>1</sub>-DPLL is extensive for extraction of carrier phase from the received signal [1-5].

The following points about a second order ZC<sub>1</sub>-DPLL can be revealed from earlier works reported in literature. (i) The system dynamics of a second order ZC<sub>1</sub>-DPLL is sensitive to the initial value of the state variables [5, 7, 14]. Depending on initial value of the state variables, the loop may get locked either to the same frequency as the frequency of the incoming signal to the DPLL (i.e. proper acquisition of the signal), or to the double or half frequency of the incoming signal to the DPLL, or there may be period-4 oscillation [8]. By double frequency locking we mean, in the locked state of the loop, the frequency of the digitally controlled oscillator (DCO) is exactly double as of that of the incoming signal, and similarly in half frequency locking case DCO frequency is half of the incoming signal.. (ii) The choice of the loop design parameters is a critical issue to get a stable locked state of the loop and at the same time convergence time to steady state of the loop is also dependent on loop design parameters [1, 2, 5-8, 10]. (iii) When there is jitter with the signal in the input, the period-4

oscillation reported in [5, 7, 14] becomes nonexistent, and the loop gets locked either to the double or half or the same frequency of the incoming signal to the DPLL depending on initial value of the physically controllable state variables [8]. (iv) The boundary region of initial condition leading to same frequency locking and double frequency locking, or same frequency locking and half frequency locking is not smooth; this region is very much sensitive to the initial condition. Or in other words the basin of attraction of proper signal acquisition is of fractal nature. In these regions the Lyapunov exponent is positive. (v) The loop has a finite frequency acquisition range (FAR), bounded on both side of the loop nominal frequency ( $f_0$ ), determined by loop parameters [6 & 8].

In this paper a modified structure of a second order ZC<sub>1</sub>-DPLL, called MSODPLL has been proposed to extend the lock range. The modification algorithm is to provide initial sum to the accumulator of the digital filter of a second order ZC<sub>1</sub>-DPLL and to incorporate quick convergence unit like [9] in the conventional loop. This proposed MSODPLL is almost similar to the modified structure used in [10 & 12]. In [10] quick acquisition of the loop was established, whereas in [12] authors established the extension of limit before bifurcation of the steady state phase error. So from earlier works it is found that the modified structure has the merit of small converging time and better stability range. The aim of this paper is to establish the merit of extension of the FAR of the modified structure. Determination of acquisition properties of the loop analytically is very tough, if not impossible. So we relied on simulation results of the loop acquisition process. In section II the system equation of the loop has been shown. In section III the simulation results of the acquisitions of the conventional and modified have been shown. As the phase error dynamics of a second order ZC<sub>1</sub>-DPLL is sensitive to the initial value of the state variables, the nature of the process of convergence of a second order ZC<sub>1</sub>-DPLL can also be tested by examining the Lyapunov exponents from the discrete phase errors developed in the process of signal acquisition. Therefore to test the process of convergence, Lyapunov exponents from the large number of loop phase error sequences were calculated. In section IV the Lyapunov exponents were calculated from discrete phase errors as developed in both type of the loop. From all these the superiority of the modified structure over the conventional loop in respect of lock range or frequency acquisition range (FAR) has been established.

II. SYSTEM MODEL

Fig 1 gives the block diagram of the conventional second order ZC<sub>1</sub>-DPLL (CSODPLL). The input signal to the DPLL Asin(ωt + θ(t)) has been sampled by the pulses from the digitally controlled oscillator (DCO), the algorithm of which is given by

$$T(k+1) = T_0 - y(k) = t(k+1) - t(k) \quad (1)$$

Where T<sub>0</sub> is the DCO nominal period and y(k) is the output of the loop digital filter (LDF) at the k-th sampling instant at t(k).

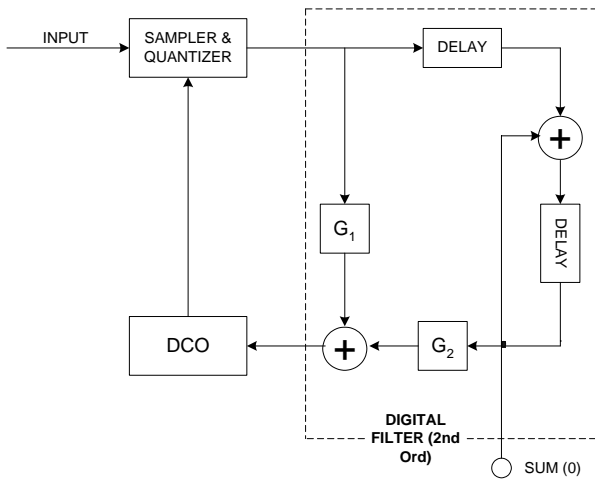


Figure 1 Block diagram of a CSODPLL with SUM as initial control parameter.

In terms of the LDF parameters (G<sub>1</sub> and G<sub>2</sub>) and sampler output (Asinφ(k)), the LDF output y(k) is given as

$$y(k) = (G_1 + G_2)Asin\phi(k) + G_2A \sum_{i=0}^{k-1} sin\phi(i) \quad (2)$$

Where φ(k) is the loop phase error defined as

$$\phi(k) = (\omega - \omega_0)t(k) + \theta(t(k)) - \omega_0 \sum_{i=0}^{k-1} y(i) \quad (3)$$

Now we define a state variable SUM (k) as

$$SUM(k) = \sum_{i=0}^{k-1} sin\phi(i) \quad (4)$$

This is proportional to the content of the accumulator arm of the LDF. Then the phase governing equation of the system can be had as

$$\phi(k+1) = 2\pi(\xi-1) + \phi(k) - \xi(K_1+K_2)sin\phi(k) - K_2\xi SUM(k) \quad (5)$$

where ξ = ω/ω<sub>0</sub> the signal detuning, K<sub>1</sub>= G<sub>1</sub>Aω<sub>0</sub> and K<sub>2</sub> = G<sub>2</sub>Aω<sub>0</sub>. The phase error dynamics for a given loop (K<sub>1</sub> & K<sub>2</sub>) with an incoming signal ω (i.e. given ξ) can be examined with (5) for a set of variable with initial φ(0) and SUM (0).

From (5) one can come to the phase governing equation as in [5] by taking the difference two consecutive phase errors

$$\phi(k+2) = 2\phi(k+1) - \phi(k) - \xi K_1 r sin\phi(k+1) + \xi K_1 r sin\phi(k) \quad (6)$$

Where r = 1 + K<sub>2</sub>/K<sub>1</sub>. The phase error dynamics for the loop can also be studied from (6) as in [5]. It is easy to show that if iteration of (6) converges, the steady state phase error φ(k) is zero, i.e. the sampler output Asinφ(k) is equal to zero. Thus if a locked state is achieved there is no phase error between the incoming signal and DCO signal. Therefore in the phase locked condition of a second order DPLL the DCO output is in same phase with the input signal, i.e. the steady state phase error φ(ss) is 0. In this situation the DCO control signal is provided by the accumulator, and its final output value SUM(ss) is given by

$$SUM(ss) = (2\pi/\omega_0 - 2\pi/\omega) / K_2 \quad (7)$$

Now let us come to the structure of the proposed MSODPLL. Fig 2 gives the block diagram of the MSODPLL. The structure of the MSODPLL is almost similar to CSODPLL except an additional weighted error signal (difference between signal samples of the present and the previous sampling instant) has been added to the signal sample. In addition it has been considered that initial SUM can be given as an input in a MSODPLL. If we make the weight factor P equal to zero the modified loop becomes a CSODPLL. This logic is almost similar to the logic used in quick response DPLL proposed by authors in [9, 10]. Therefore the input to LDF in a MSODPLL at the k-th instant is

$$Asin\phi(k) + P\{Asin\phi(k) - Asin\phi(k-1)\} \quad (8)$$

When P is equal to zero the loop becomes the conventional loop, i.e. a CSODPLL.

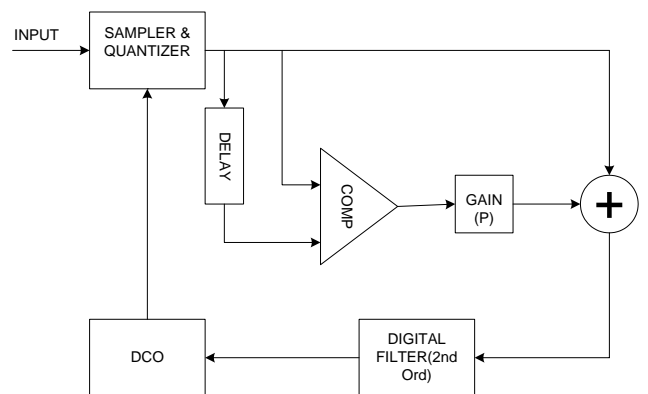


Figure 2 Block diagram of MSODPLL.

Following same procedure as above the phase governing equation of MSODPLL can be had as

$$\phi(k+2) = 2\phi(k+1) - \phi(k) - \xi K_1 r(1+P) sin\phi(k+1) + \xi K_1 \{1 + (r+1)P\} sin\phi(k) + \xi K_1 P sin\phi(k-1) \quad (9)$$

It is easy to note that when P = 0, eqn.(9) reduces to eqn.(6)

Equation (5) is more physical for studying the phase error dynamics of a CSODPLL, as both the initial condition is externally controllable. However in this paper we have studied the dynamics using the real time simulation of the system rather than the system equation.

III. SIMULATION RESULTS

The dynamics has been observed by simulating the system in real time in a digital computer. In our case the system was simulated by simulating each individual building block in real time in a digital computer. Then the time development of the loop phase errors for a given loop ( $K_1$  &  $K_2$ ) was noted by noting the S/H output and hence the loop phase error. The phase error  $\phi(k)$ 's taken as modulo  $2\pi$  quantity within  $-\pi$  to  $\pi$  because of the sinusoidal non linearity term in the system equation. The upper limit of initial value of SUM(0) is specified from physical consideration that the (k+1)-th SI should be later than k-th SI and so from (1) SUM(0) should be less than  $(2\pi/K_2)$ .

From the simulation it is found that the steady state output from the sampler of the loop is zero in the locked state, as expected from eqn. (5) or (6). Therefore in the locked state the phase of the DCO is same as the phase of incoming signal and its increment in each step is  $2\pi$ . The dots in figure 3 represents the ranges of initial condition ( $\phi(0)$  and SUM(0)) leading to the locked state of the CSODPLL with  $K_1$  &  $K_2 = 1$ . Loop parameters  $K_1$  &  $K_2 = 1$  produce fastest acquisition in a CSODPLL [1, 5, 7]. In this case of the locked state the SUM value and its increment is zero. From the figure it is found that the loop converges to steady state for both positive and negative values of initial SUM for entire ranges of PHI ( $\phi$ ) between  $-\pi$  to  $\pi$ .

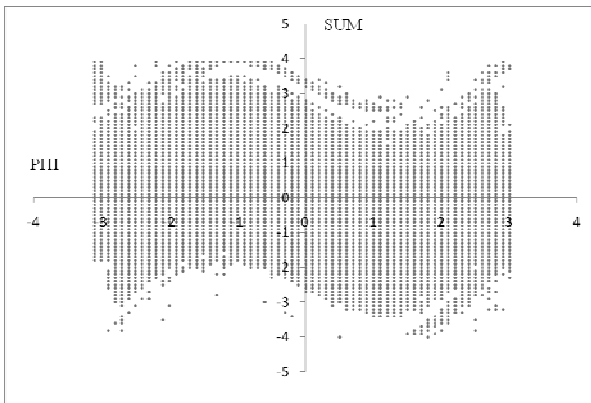


Figure 3. Ranges of initial condition of a second order ZC1-DPLL leading to same frequency locking for  $\xi=1$

Taking zero initial SUM, the ranges of  $\xi$  leading to proper acquisition of the signal i.e. same frequency locking of a CSODPLL (with different  $K_1$  &  $K_2$ ) have been found out from the simulation. This gives us the FAR of the loop. Figure 4 shows the variation of FAR with loop parameter. From figure 4 we can see upper limit of  $\xi$  as well as ranges of  $\xi$  is decreasing with increasing  $K_1$ , i.e. FAR is less [5,8]. From the following simulation we want show that using MSODPLL we can increase the FAR.

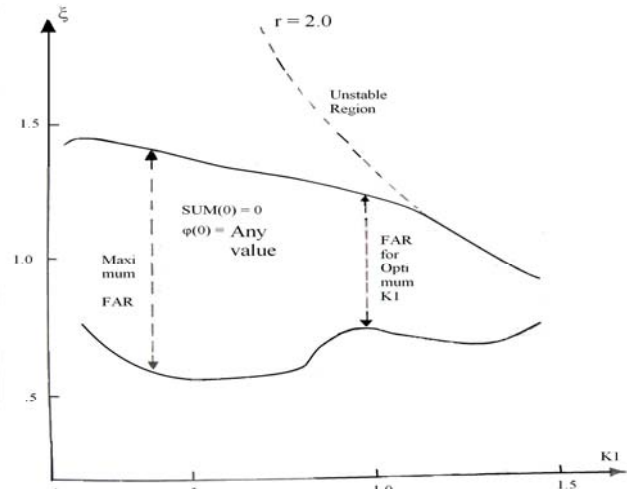


Figure 4. Simulated Lock Range of a CSODPLL.

From figure 5 it is easy to note that a CSODPLL (with loop parameter  $K_1$  &  $K_2 = 1.2$ ) does not converges to steady state for signal detuning value  $\xi = 1.2$  in large portion of initial values of the state variables (PHI and SUM).

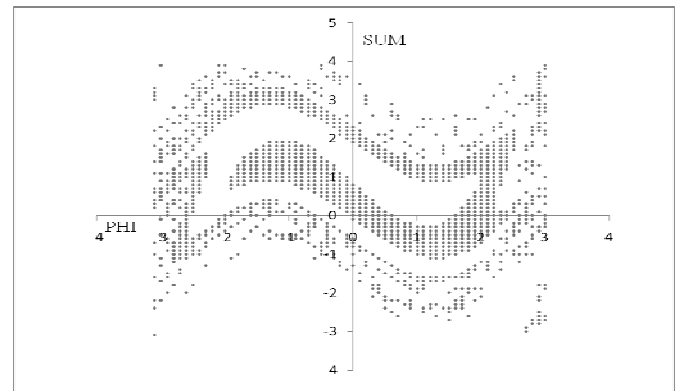


Figure 5. Ranges of initial condition of CSODPLL with  $K_1$  &  $K_2 = 1.2$  leading to frequency locking for  $\xi=1.2$

But a MSODPLL with same parameter values converges to steady state in the large portion of initial values of the state variables. This can be found from figure 6.

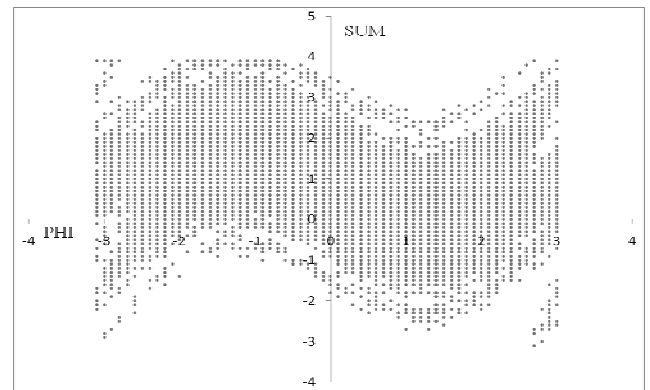


Figure 6. Ranges of initial condition of MSODPLL with  $K_1$  &  $K_2 = 1.2$  and  $P = -0.1$  leading to frequency locking for  $\xi=1.2$

Similarly figure 7 shows that a CSODPLL (with loop parameter  $K_1$  &  $K_2 = 1.2$ ) does not converges to steady state

for signal detuning value  $\xi = 0.8$  in the large portion of initial values of the state variables.

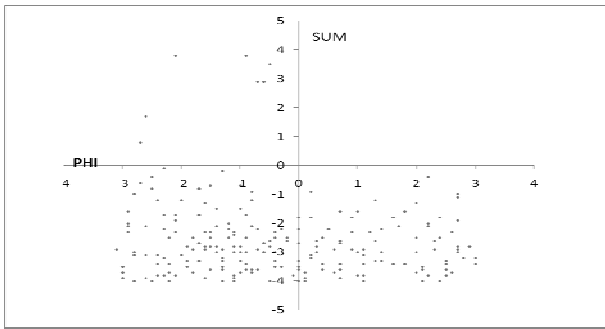


Figure 7. Ranges of initial condition of CSODPLL with  $K_1$  &  $K_2 = 1.2$  leading to frequency locking for  $\xi = 0.8$

But a MSODPLL with same parameter values and same detuning as in fig. 7 converges to steady state in the large portion of initial parameter values. This can be seen from fig.8. Similar results were obtained from the simulation with other values of loop parameters and signal detuning.

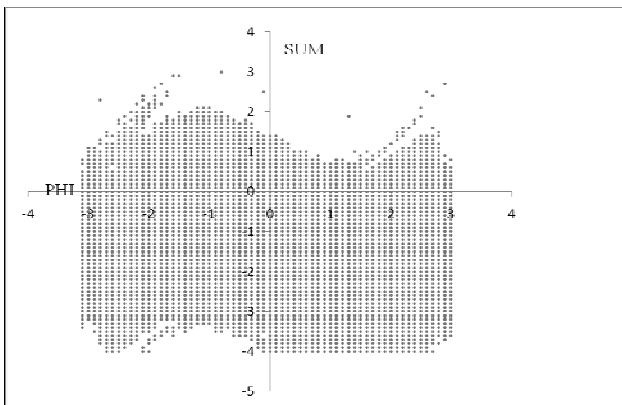


Figure 8. Ranges of initial condition of MSODPLL with  $K_1$  &  $K_2 = 1.2$  and  $P = -0.1$  leading to frequency locking for  $\xi = 0.8$

These ranges of initial condition leading to frequency locking are very important as it determines the range of frequency that can be acquired by a second order CSODPLL or MSODPLL. Therefore from Fig 5 – 8 we can conclude that a MSODPLL can acquire signal with larger limit of  $\xi$  than a CSODPLL, i.e. FAR is larger for MSODPLL

#### IV. STUDY OF LYAPUNOV EXPONENTS

Lyapunov exponents are most useful diagnostic for the system having strong dependence on initial conditions (i.e. chaotic system). Lyapunov exponents are the average exponential rates of divergence or convergence of nearby orbits in phase space. Using the technique of [15] for each initial condition in a loop the Lyapunov exponent was determined from large no of phase errors developed in the process. This process was repeated for all other initial conditions. The Lyapunov exponents are determined from large number of discrete phase errors of CSODPLL with different values of  $K_1$  &  $K_2$  and all possible  $\phi(0)$  and  $SUM(0)$

as initial condition. The regions of positive Lyapunov exponents, i.e. the regions not producing the locked state of the loop were found out. These are represented as dots (.) in phase plane plot. So a dot in the plot means it does not produce the locked state.

Similar processes have been repeated for determining the Lyapunov exponents of MSODPLL with same  $K_1$  &  $K_2$  and  $P = -0.1$ . Figure 9 through 11 shows such plots of positive Lyapunov exponents of CSODPLL and MSODPLL with all possible initial values of the loops.

Fig. 9 shows initial values of phase variables to a CSODPLL leading to positive values of Lyapunov exponents. It is easy to find from the figure that major portion of the ranges of initial conditions is unstable i.e. it does not produce the locked state of the loop.

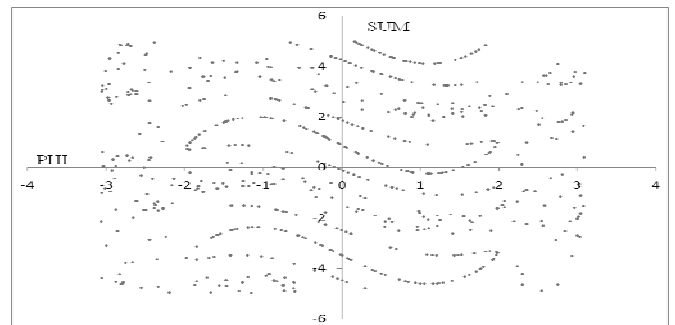


Figure 9. Ranges of initial condition of CSODPLL with  $K_1$  &  $K_2 = 1.2$  leading to +ve Lyapunov expo for  $\xi = 1.2$

Whereas in figure 10 one can easily find that in a MSODPLL with same detuning value produce locked state in larger ranges of initial values of the variables.

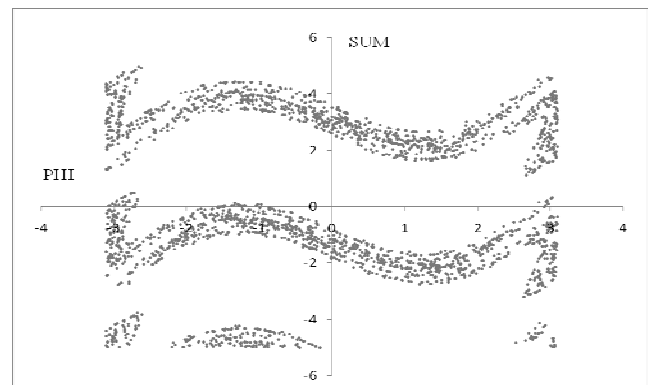


Figure 10 Ranges of initial condition of MSODPLL with  $K_1$  &  $K_2 = 1.2$  and  $P = -0.1$  leading to +ve Lyapunov expo for  $\xi = 1.2$

Figure 11 clearly shows that larger ranges of initial conditions produce locked state in a MSODPLL.

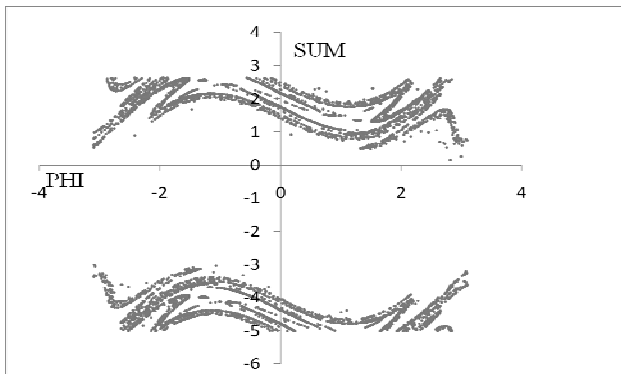


Figure 11. Ranges of initial condition of MSODPLL with  $K_1$  &  $K_2 = 1.2$  &  $P = -0.1$  leading to +ve Lyapunov expo for  $\xi = 0.8$

Therefore from this study we find that the region of convergence to the locked state i.e. the basin of attraction to the locked state is more in a MSODPLL than in a CSODPLL. So one can easily conclude that MSODPLL converges to locked state with larger ranges of frequencies than a CSODPLL.

## V. CONCLUSIOS

Simulation study clearly shows that MSODPLL with same values of loop parameter converges to the locked state with larger ranges of signal detuning value  $\xi$  than a CSODPLL. Therefore the lock range is more in a MSODPLL than a CSODPLL. So MSODPLL is more suitable in communication systems where larger bandwidth is required like FH spread spectrum etc.

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