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High-Performance Generalized ADPWM Algorithm for VSI Fed IM Drives for Reduced Switching Losses

K. Sri Gowri[1], T. Brahmananda Reddy[2], and Ch. Sai Babu[3]
[1]E.E.E Department, RGMCET, Nandyal, Kurnool, A.P, India
Email: gowrivasu.3@gmail.com
[2]E.E.E Department, G. Pulla Reddy Engineering College, Kurnool, A.P, India
Email: tbnr@rediffmail.com
[3]E.E.E Department, JNTUK, Kakinada, A.P, India
Email: chs_eee@yahoo.co.in

***Abstract*— In this paper a high performance generalized advanced discontinuous pulse width modulation (ADPWM) algorithm for voltage source inverter (VSI) fed induction motor drives is proposed. The proposed ADPWM method uses two categories of DPWM sequences, 012, 721, 0121 and 7212 which not only reduces the inverter switching losses but also reduces the line current distortion during medium to high speed operations. However analysis in this paper is limited to inverter switching losses. In this paper it is shown that, utilizing a set of DPWM sequences and by changing the zero state at any spatial angle $\alpha = \gamma$ where γ is between 0^0 and 60^0an infinite number of ADPWM methods can be generated which are categorized as "continual clamping" and "split clamping" sequences. It will be shown analytically and through simulation that nearly 40% reduction in inverter switching losses and 36% reduction in steady state line current distortion (compared with the CSVPWM) can be achieved with the proposed ADPWM methods at high power factor loads.**

***Index Terms*— ADPWM, Continual clamping, CSVPWM, Split clamping, inverter switching losses, normalized switching loss**

I. INTRODUCTION

VSI inverter fed induction motors are widely used in industry due to their simplicity and ruggedness. These motors can be fed from Current Source Inverters (CSI) or Voltage Source Inverters (VSI), and used as variable speed drives. Recent advances in semiconductor technology have led to new generations of fast-acting, power semiconductor switches like GTOs, MOSFETs, IGBTs, and more recently, IGCTs. The performance and characteristics of these switches strongly favour the VSI topology over the CSI one. This has been a major reason for VSI fed induction motor drives becoming more popular than CSI fed ones. PWM strategies are required for switching the devices in a VSI appropriately to generate variable voltage, variable frequency, 3-phase AC required for the variable speed induction motor drive. The performance of the drive strongly depends on the Pulse width Modulation (PWM) technique employed. At high power levels, the inverter can switch only at low frequencies, and the harmonic distortion is quite high. Hence, PWM strategies for high-power drives must aim in reducing the inverter switching losses, harmonic distortion, subject to low switching frequencies of the inverter. Development and analysis of such PWM strategies are carried out in this paper.

In recent years several PWM methods have been developed to reduce the current ripple and to get constant switching frequency. One of such method is space vector PWM (SVPWM) method [1]-[4]. In this method for each sampling period reference voltage vector demanded by the PWM inverter has been generated in an average sense and is used for the further analysis. However SVPWM gives inferior performance at higher modulation indices. Moreover, as the SVPWM is a continuous PWM (CPWM) method the switching losses of the inverter are also high. Hence to reduce the switching losses and to improve the performance of the drive at high modulation region several DPWM methods have been reported in [1]-[5]. In this paper an ADPWM algorithm is proposed which uses two categories of DPWM sequences, 012, 721, 0121 and 7212. First two are termed as clamping sequences and the last two are termed as double switching clamping sequences. The proposed methodology generalizes the ADPWM algorithm that uses these two categories of sequences using a zero voltage vector distribution variable, σ so that choosing a proper value for σ generates the required DPWM sequence thereby giving scope for the ease in implementing the generalized ADPWM algorithm. DPWM sequences can be used effectively to reduce either the switching losses or the harmonic distortion as may be required. With the proposed method it is shown that different ADPWM methods can be generated, which shows significant reduction in inverter switching losses as well as line current distortion. This ultimately proves that compared with CSVPWM the proposed ADPWM method gives better performance in terms of inverter switching losses as well as line current distortion.

II. SVPWM BASED SWITCHING SEQUENCES

The space vector approach has become very popular over the last decade. In this approach, the reference is provided as a voltage space vector, which is sampled once in every sub cycle and an average vector equal to the sampled reference vector is generated by timeaveraging of the different voltage vectors produced by the inverter [6].

According SVPWM algorithm the reference voltage vector is synthesized in an average sense using two near by active voltage vectors and two zero voltage vectors. With a three-phase voltage source inverter (VSI) there are eight possible switching states. The two states, from which no power gets transferred from source to load are termed as null vectors or zero states. The other six states called active states.

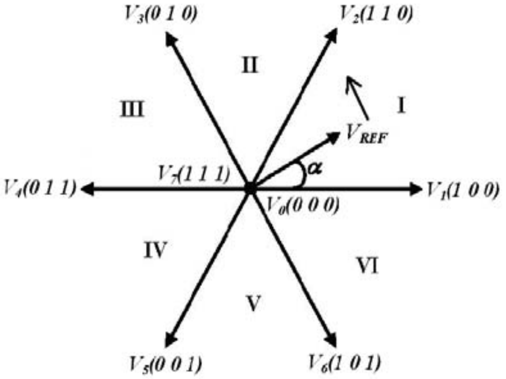


Figure 1. Switching states and corresponding voltage vectors of a three phase VSI. I, II, III, IV, V, VI are the sectors.

It can be shown that all the six active states can be represented by space vectors given by (1) forming a regular hexagon dividing the space plane into six equal sectors denoted as I, II, III, IV, V, VI shown in Fig.1.

$$V_k = \frac{2}{3} V_{dc} * e^{j(k-1)\frac{\pi}{3}}, k = 1,2,...,6. \tag{1}$$

For a given reference voltage V_{REF} making an angle α with reference to V_1 in first sector, the volt-time balance is maintained by applying the active state1 V_1, active state2 V_2 and two zero states V_0 and V_7 together for durations, T_1, T_2 and T_Z respectively, as given in (2)[6].

$$T_1 = M * \frac{\sin(60^o - \alpha)}{Sin 60^o} * T_s \tag{2.1}$$

$$T_2 = M * \frac{\sin \alpha}{\sin 60^o} * T_s \tag{2.2}$$

$$T_Z = T_s - T_1 - T_2 \tag{2.3}$$

where 'M' is the modulation index, given by $M = \frac{3V_{REF}}{2V_{dc}}$.

Although according to CSVPWM strategy the two active vectors and two zero vectors must be applied for durations as in (2), these can be applied in different ways to generate different sequences. The rules that followed in SVPWM algorithm to synthesize the reference voltage vector are the nearest active voltage vectors must be applied, in every switching only one state should transform and in every sub cycle the sequence has to end up with same switching state that it starts with. Categorizing the sequences is based on these factors. First one is if two active states and two inactive states are used it is categorized as CSVPWM sequence, Second category is based on the fact that the total T_Z can be spent in either V_0 or V_7 state. The resultant sequences are 012,721 which are referred in this paper as clamping or DPWM sequences for the reason that one of the phase clamps to either of the bus in a sub cycle and its modulating waveforms are discontinuous. Lastly, based on the division of either of active voltage vectors duration the sequences are categorized as double switching bus-clamping sequences or double switching DPWM sequences, examples of which are 0121,7212,2721,1012. Since 2721, 1012 gives high ripple during high modulation regions, they are not considered in further discussions. The considered switching sequences are shown in Fig.2 assuming the reference vector position in sector I.

A. *Proposed ADPWM methods*

In this paper to utilize the freedom of dividing the zero state duration a zero voltage vector distribution variable σ is used to divide the zero state time between two zero states and are defined by (3).

$$T_0 = T_Z \sigma \tag{3.1}$$

$$T_7 = T_Z (1 - \sigma) \tag{3.2}$$

In DPWM methods the total zero state duration is spent in only one of the two zero states. Hence for, $\sigma = 0$, T_0 becomes zero which ultimately says that the total zero state duration is spent in V_7 or in other words represents 721 or 7212 sequences and similarly for $\sigma = 1$, T_7 becomes zero which conveys that the total zero state duration is spent in V_0 or in other words represents 012 or 0121 sequences . In [6], [9] by varying a single constant variable a generalized DPWM algorithm utilizing the freedom of dividing the zero state time within a sampling period is used to generate different DPWM methods.

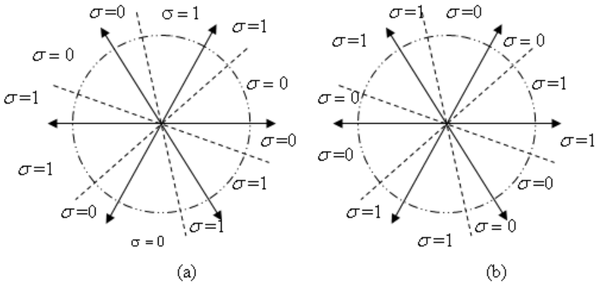
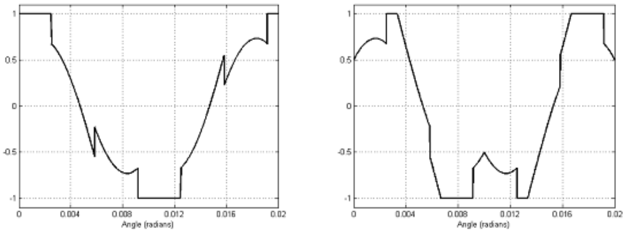


Figure 2. Generation of space vector based ADPWM techniques (a) continual clamping (b) split clamping.

In the present paper the same concept is been used to generate two types of ADPWM methods. One of such approach uses clamping sequences 012 and 721, and the other approach uses double switching clamping sequences 0121 and 7212. The similarity between these two approaches is that both generate discontinuous PWM sequences in which one of the three phases clamp to either of the buses for sub cycle duration and the contrast characteristic between these two is that in first approach which uses clamping sequences the active state duration is spent in either of the active states whereas in second approach which uses double switching clamping sequences the total active state duration is divided into two equal halves and applied twice in very sub cycle, which results not only clamping of one of the phases but also switches twice the remaining one of the two phases, for the reason why these sequences are termed as double switching clamping sequences.

To generalize ADPWM methods and to generate ADPWM methods in either of the two approaches, the constant variable σ can be applied at any spatial angle γ to yield different DPWM methods and when in case of continual and split clamping methods with $\gamma \neq 30^0$ it results in ADPWM methods, i.e. two sequences 012 and 721 or 0121 and 7212 were used in each sector according to the set policy, which generates continual and split clamping methods as shown in the Fig.3. The same methodology results in the existing DPWM methods, well known by the names DPWM1, DPWM3 for $\gamma = 30^0$ [6], [7] and for $\gamma = 0^0 or 60^0$ it results in the existing DPWM methods renowned by the names DPWM2 and DPWM0[6], [7].

It is observed that the modulating waveforms of continual and split clamping do not differ with the clamping and double switching clamping sequences [6],[10]. The modulating waveforms of the above said methods are shown in Fig.3 for $\gamma = 45^0$.



(a) (b)

Figure 3. Modulating waveforms of (a) continual clamping and (b) split clamping with $\gamma = 45^0$.

III. ANALYSIS OF INVERTER SWITCHING LOSSES

The present section deals with the analysis of inverter switching losses. *The switching losses in a PWM-VSI depend on load current and increase with load current magnitude.* As in the case of continuous PWM (CPWM) methods all the three phases commutate in every switching cycle, and so the switching losses are the same for all CPWM and are independent of the phase angle. But, in the case of DPWM methods as every phase clamps for a period of 120^0 the switching losses are comparatively reduced by a factor of one third (when compared with CPWM method) and are merely influenced by the factors like modulation method and load power factor angle [8]. For this reason different ADPWM methods show variation in switching losses with the variation in load power factor. Since, the modulating wave decides the period for which a phase clamps and the instant of clamping, selection of particular ADPWM method can simultaneously reduce the load current ripple and switching losses significantly which further contributes for the efficiency and performance of the drive. With the proposed GADPWM algorithm it is possible to change the position and or period of clamping by varying a single variable thus creating ease in applying different DPWM methods as per the requirement. Also, it will be useful to characterize and compare the switching losses of different ADPWM methods.

Considering only the fundamental component of the phase current (i_1) and assuming that the inverter switching devices has linear turn on and turn off characteristics, the switching energy loss in an inverter leg is proportional to the phase current and the number of switching of that phase(n) in each sector. The normalized switching energy loss (E) is defined in (4). I_m and ϕ are the peak phase current and line side power factor angle respectively. The average of E $\left(E_{avg}\right)$over a fundamental cycle gives the average switching energy loss per sub cycle. From [11], [12] it can be concluded that in addition to the type of clamping, the period of clamping which in turn influenced by the value of γ plays important role in reducing E. Ref. [11], [12] also concludes that continual clamping with $\gamma = 30^0$ is better at power factors close to unity and split clamping with $\gamma = 30^0$ is better at power factors close to zero in terms of E.

$$E = \frac{n|i_1|}{I_m} = n|\sin(wt - \phi)| \qquad (4.1)$$

Inverter switching loss is obtained by multiplying E_{avg} with the number of sub cycles per second, the sampling frequency$\left(f_s\right)$.The generalized expression for normalized inverter switching loss SWL_{norm} for a given PWM sequence is defined by (5), in which f_{sw} is the switching frequency which is taken as 5KHz for simulation. The sampling frequency is $2f_{sw}$ for CSVPWM sequence and clamping sequences and it is $3f_{sw}$ for double switching clamping sequences. Expressions for normalized switching loss corresponding to CSVPWM sequence, clamping sequence based continual clamping, clamping sequence based split clamping, double switching clamping sequence based continual clamping and double switching clamping sequence based split clamping can be derived using (5)[10].

$$SWL_{norm} = \frac{E_{avg}}{\left(2/\pi\right)}\frac{f_s}{f_{sw}} \qquad (5)$$

Observations from Fig.4 and Fig.5 lead to a conclusion that up to 53.7^0 power factor angle continual clamping and beyond 53.7^0 power factor angle split clamping with

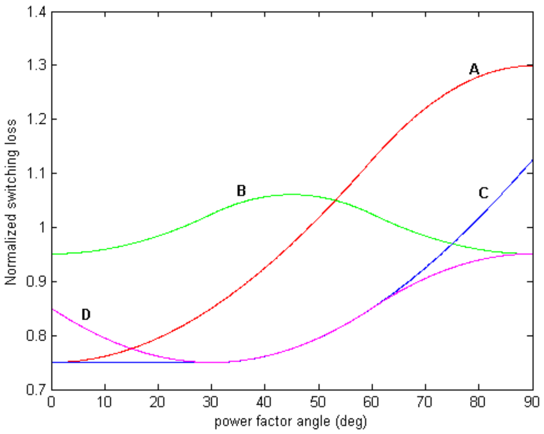


Figure 4. A-continual clamping using clamping sequences with $\gamma = 30^0$, B- split clamping using clamping sequences with $\gamma = 30^0$, C- continual clamping using clamping sequences with optimal γ, D- split clamping using clamping sequences with optimal γ.

$\gamma = 30^0$ confer minimum switching losses. Executing a given PWM method with optimal γ in terms of minimum switching losses can reduce switching losses at all power factors. Equations for optimal γ in each interval can be found by equating the derivative of the respective function to zero [10]. Executing the continual clamping PWM method with optimal γ generates the C and C' in Fig.4 and Fig.5 respectively. Similarly executing split clamping PWM method with optimal γ generates D and D' in Fig.4 and Fig.5 respectively. Curve C in Fig.4 or curve X in Fig.6 are referred as "generalized discontinuous PWM" in [7]. Further reduction in switching losses can be achieved by executing ADPWM using clamping sequences with optimal γ, as shown by curve Y in Fig.6 For loads whose power factor angle varies between -30^0 to +30^0, further more reduction in switching losses can be achieved by executing ADPWM using double switching clamping sequences with optimal γ, as shown by curve Z in Fig.6. Assuming the load to be an induction motor in which source power factor angle generally varies from 20^0 to 30^0 lagging, and for a given switching frequency, compared with CSVPWM method nearly 25% reduction in switching losses can be achieved with the ADPWM method using clamping sequences and nearly 36.56% reduction in switching losses can be achieved with the ADPWM method using double switching clamping sequences.

IV. SIMULATION RESULTS

Simulation was done in MATLAB/Simulink using the Runge-kutta solver, with a fixed step of 10 μ sec on a 1.5KW, 1440rpm, four pole, 3-ϕ V/f controlled induction motor drive having the following parameters: Rs=7.83Ω, Rr=7.55Ω, Ls=0.4751H, Lr=0.4751H, Lm= 0.45351H, J=0.06Kg.m^2. Simulation results shows that compared with CSVPWM simultaneous reduction in inverter switching losses as well as harmonic distortion in steady state line current is achieved with the proposed ADPWM method to an extent shown in Table I.

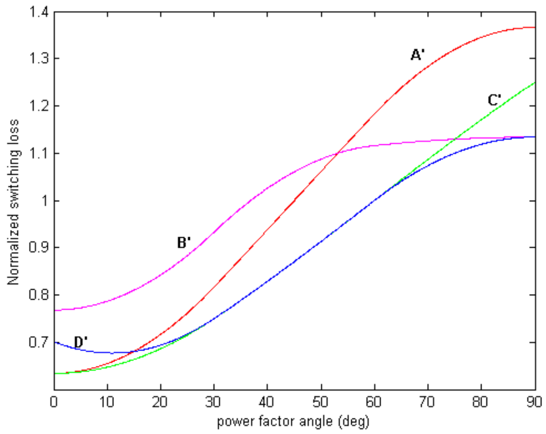


Figure 5. A-continual clamping using double switching clamping sequences with $\gamma = 30^0$, B- split clamping using double switching clamping sequences with $\gamma = 30^0$, C- continual clamping using double switching clamping sequences with optimal γ, D- split clamping using double switching clamping sequences with optimal γ.

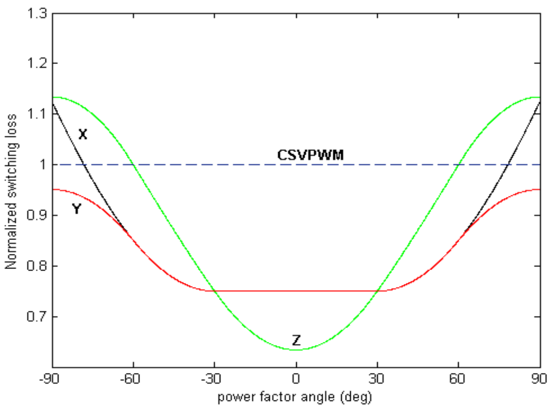


Figure 6. Normalized switching loss against power factor angle for different PWM methods. Curve X -Generalized discontinuous PWM, Curve Y- Clamping sequences based ADPWM, Curve Z- Double switching clamping sequences based ADPWM.

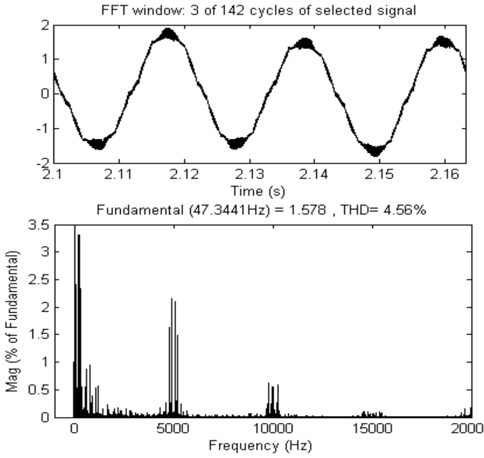


Figure 7. No-load current (A) and harmonic spectra with CSVPWM sequence at a modulation index of 0.82, $f_s = 5KHz$.

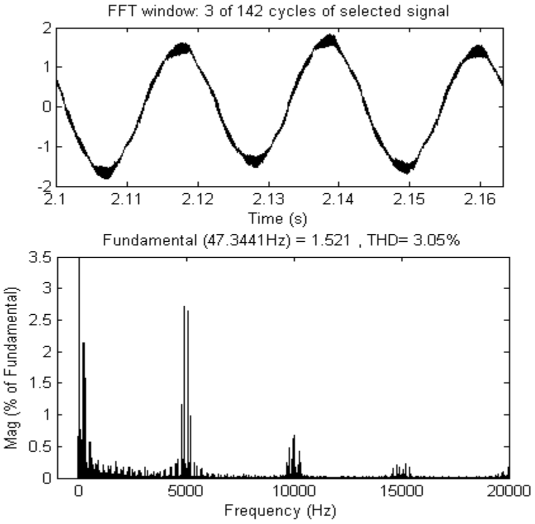


Figure 8. No-load current (A) and harmonic spectra with clamping sequences based ADPWM sequence at a modulation index of 0.82, $f_s = 5KHz$.

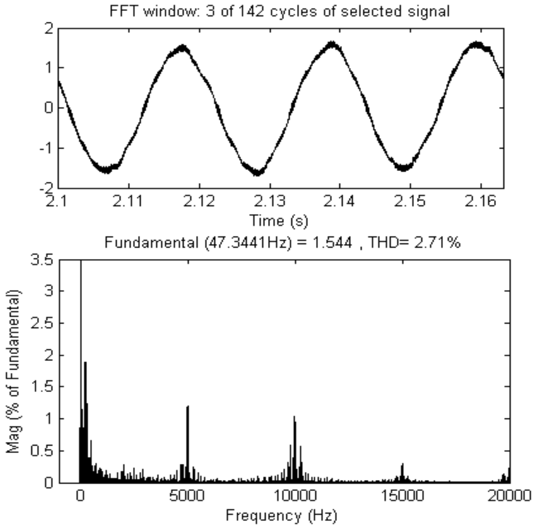


Figure 9. No-load current (A) and harmonic spectra with double switching clamping sequences based ADPWM sequence at a modulation index of 0.82, $f_s = 5KHz$.

V. CONCLUSIONS

The paper presents a generalized ADPWM algorithm that deal with a class of DPWM sequences. Based on the switching of a phase the considered DPWM sequences were classified into two categories, clamping and double switching clamping sequences. Using these two sets of sequences a generalized ADPWM algorithm is proposed which gives optimal performance both in terms of line current distortion and inverter switching losses. Further the role of the position and period of clamping is lime lighted. Finally it is concluded from the work that selection of suitable clamping method can reduce the line current distortion and inverter switching losses to a considerable extent. Justification is done by comparing the simulation results with CSVPWM method.

TABLE I
%REDUCTION IN THD AND SWL_{norm}

	% Reduction	
	Harmonic Distortion	SWL_{norm}
CSVPWM	Zero	Zero
ADPWM(clamping)	33.11	25
ADPWM(double switching clamping)	40.57	36.56

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