

# New Hybrid 27 Level Multilevel Inverter fed Induction Motor Drive

K.Ramani<sup>1</sup>, A.Krishnan<sup>2</sup>

<sup>1</sup>K.S.Rangasamy College of Technology, Tiruchengode. India 637215  
Email: [kreee82@gmail.com](mailto:kreee82@gmail.com)

<sup>2</sup>K.S.Rangasamy College of Technology, , Tiruchengode. India 637215  
Email: [a\\_krishnan26@hotmail.com](mailto:a_krishnan26@hotmail.com)

**Abstract**— This paper deals with new hybrid multilevel inverter fed induction motor drive. It focuses on asymmetrical topologies, the general function of this multi level inverter is to synthesize a desired voltage from several separate dc source. This hybrid topology has more advantageous of industrial applications. In conventional methods, the need of converters to supply the cells of reversible multilevel converters increases the cost and losses of such inverters. The proposed method introduces 27 levels Inverter fed Induction Motor drive. With the use of high level inverter, resolution is increase and also the harmonics is highly reduced.

**Index Terms**— AC Drive, Multi level Inverter, Total Harmonics Distortion (THD), DC link voltage.

## I. INTRODUCTION

The multilevel inverter has introduced a solution to increase the converter output voltage above the voltage limits of classical semiconductors. There are quite a lot of ways to achieve multilevel inverters [1]-[5]. The most important topologies are the neutral point clamped inverters, the flying capacitors and the cascade inverters. This paper investigates new hybrid multilevel inverter which significantly increase the level number of output waveforms and thereby dramatically reduces the low order harmonics and total harmonics distortion [2].

Moreover the stage with higher DC link voltage has less switching frequency and therefore reduced switching losses. They also allow combining different types of switches to optimize the inverter efficiency [6].The new hybrid multilevel inverter consists of full bridge modules which have the relationship of  $1v, 3v, 9v, \dots, 3^{s-1}v$  for dc link Voltage .The output waveform has 27 levels,  $\pm 13, \pm 12, \pm 11, \pm 10, \pm 9, \pm 8, \pm 7, \pm 6, \pm 5, \pm 4, \pm 3, \pm 2, \pm 1, 0$ .

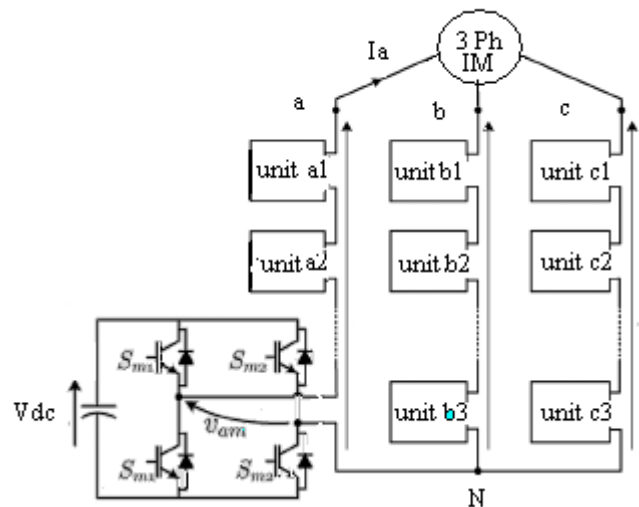


Figure 1. Basic new hybrid inverter scheme.

The inverter generates  $3^s$  different voltage levels (e.g. an inverter with  $s=3$  cells can generate  $3^3=27$  different voltage level).The basic hybrid multilevel inverter structure for one phase is illustrated in Fig 1.This multilevel inverter is made up of a set of series connected cells. Each cell consists of a 4-switch H-bridge voltage source inverter. The output inverter voltage is obtained by summing the cell contributions.

In conventional method, low level inverter is used. Better sinusoidal output was not obtained which is the drawback of the conventional system and the harmonics was high. So increase the levels of the inverter to get high resolution, hence the output wave form is mostly sinusoidal wave form.

The cascaded multilevel inverter is prepared by series connection of single phase full bridge inverter [7, 9]. The common function of multilevel inverter is to synthesize a desired voltage from several separate DC sources [10]. Each source is connected to a single phase full bridge inverter. Each inverter is capable of generating three different output voltages,  $+V_{dc}, 0$  and  $-V_{dc}$ .

K. Ramani is Senior Lecturer with Electrical and Electronics Engineering dept, K.S.Ranagasamy College of Technology, Tiruchengode. 637215 (e-mail: [kreee82@gmail.com](mailto:kreee82@gmail.com)). Mobile Number 9788 518536

Dr.A.Krishnan is Dean, K.S.Rangasamy College of Technology, Tiruchengode, 637215 , Namkkal Dt, Tamilnadu, India (e-mail: [a\\_krishnan26@hotmail.com](mailto:a_krishnan26@hotmail.com)).

II. MODELING OF MULTILEVEL NEW HYBRID INVERTER

For each full bridge inverter the output voltage is given by

$$V_{oi} = V_{dc} (S_{1i} - S_{2i}) \tag{1}$$

and the input dc current is

$$I_{dci} = I_a (S_{1i} - S_{2i}) \tag{2}$$

$i = 1, 2, 3 \dots$  (number of full bridge inverters employed).  $I_a$  is the output current of the new hybrid inverter.  $S_{1i}$  and  $S_{2i}$  is the upper switch of each full bridge inverter. Now the output voltage of each phase of the multilevel new hybrid inverter is given by

$$V_{on} = \sum_{i=1}^n V_{oi} \tag{3}$$

III. PROPOSED METHOD

In this proposed method of the inverter, has three input stages, all the three stages are alike in the construction module. All the modules are connected as new hybrid with each module having power switches.

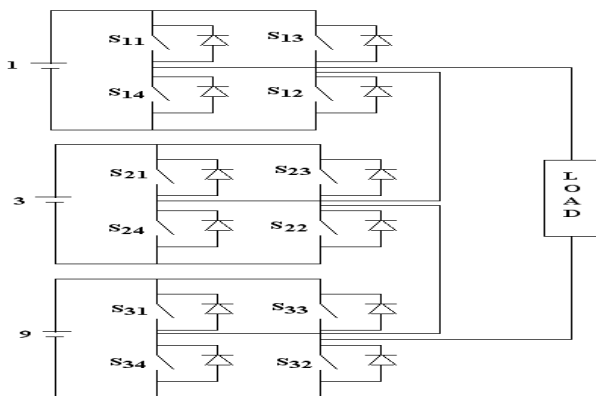


Figure 2. Proposed new hybrid inverter scheme

The power switches may be IGBT, MOSFET or any other power devices. The MOSFET's are used in this system. The power switches are operated in switching mode such that any two switches are in operating conditions at a time and other two remain in open condition. The switching is as  $S_{11}=\overline{S_{13}}$  and  $S_{12}=\overline{S_{14}}$ , this method is adopted to protect the circuit from short circuiting. The number of levels is increased by connecting maximum number of modules.

A. Inverter Resolution

The more asymmetrical configuration, the higher the resolution. The recognized number of cells, one can change the type of the cells and their supply voltages. To obtain a structure that generates identical levels, the supply voltages must examine the single-phase uniformity provision

$$\Delta U_k \leq \Delta U_{k+1} \leq \Delta U_1 + \sum_{j=1}^k (n_j - 1) \cdot \Delta U_j \tag{4}$$

Where  $U_k$  and  $n_j$  are the step and the quantity of levels of the  $k^{th}$  cell and where  $U_1$  is also the step of the resulting inverter. This condition is a function of the number of levels and of the steps of the combined cells. For the proposed structure, with one H-bridge in series the number of levels can go up to 27.

B. Single Phase Modulation Condition

MOSFET Switches of different jamming voltages are used to make up an asymmetrical multilevel inverter. So far, switches with high jamming capabilities have smaller commutation capabilities. As significance, the switching losses of the high-voltage cells are considerably increased. To play down the number of commutations of high-voltage cell, the inverter has to be considered according to a more off-putting law, the modulation condition

$$\Delta U_k \leq \Delta U_{k+1} \leq \sum_{j=1}^k (n_j - 1) \cdot \Delta U_j \tag{5}$$

An efficient multilevel inverter may be designed by using switches with low conduction losses for the high voltage cells and switches with low commutation losses for the low voltage cell. The divergence is the modulation condition for a single phase inverter.

TABLE 1  
NEW HYBRID INVERTER SWITCHING

Output voltages and switching states for the new hybrid inverter, S=3																											
Vdc	Vout																										
	-13V	-12V	-11V	-10V	-9V	-8V	-7V	-6V	-5V	-4V	-3V	-2V	-1V	0V	1V	2V	3V	4V	5V	6V	7V	8V	9V	10V	11V	12V	13V
1V	N	0	P	N	0	P	N	0	P	N	0	P	N	0	P	N	0	P	N	0	P	N	0	P	N	0	P
3V	N	N	N	0	0	0	P	P	P	N	N	N	0	0	0	P	P	P	N	N	N	0	0	0	P	P	P
9V	N	N	N	N	N	N	N	N	N	0	0	0	0	0	0	0	0	0	P	P	P	P	P	P	P	P	P

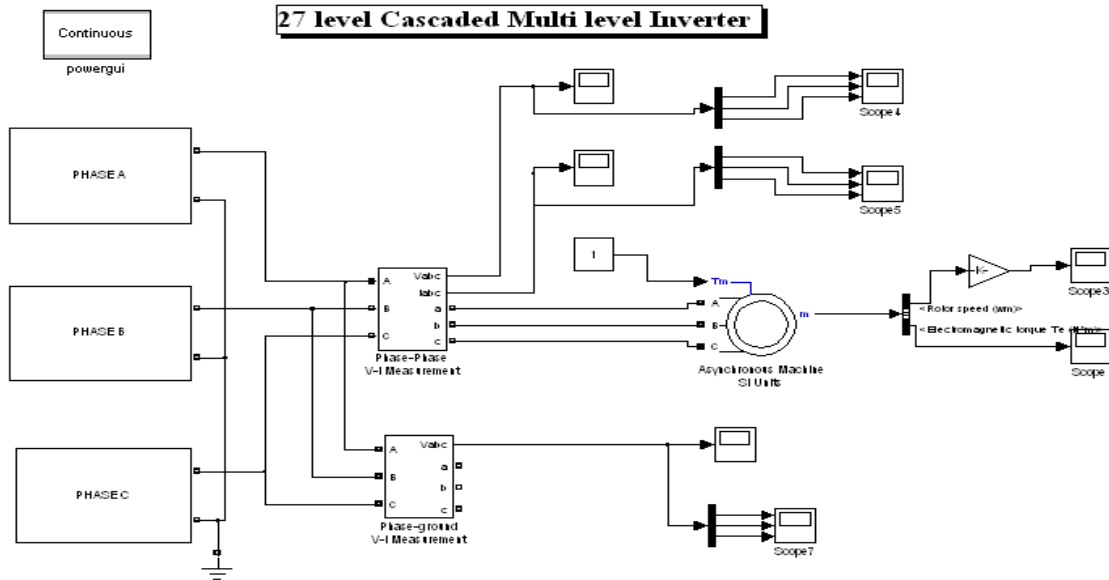


Figure 3. Simulation diagram of proposed system

Based on the conditions a number of possible input voltage combinations and the resulting number of levels, respectively for the basic structure and for the proposed structure. High voltage cells are not efficient for switching. These configurations are well-matched to generate a step stair voltage, but not for a modulated one. These solutions suit entirely for mutually modulated voltage.

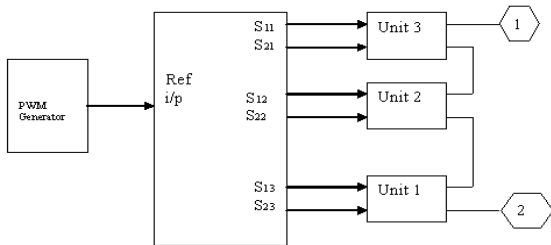


Figure 4. Simulation diagram of sub system

C. Harmonic Elimination in Multi Level Inverter

The output voltage V (t) of the multi level inverter can be expressed in Fourier series as

$$v(t) = \sum_{n=1}^{\infty} (a_n \sin n\alpha_n + b_n \cos n\alpha_n) \quad (6)$$

Due to quarter wave symmetry of the output voltage the even harmonics are absent ( $b_n = 0$ ) and only odd harmonics are present.

The amplitude of the  $n^{th}$  harmonic  $a_n$  is expressed only with the first quadrant switching angle  $\alpha_1, \alpha_2, \alpha_3, \dots, \alpha_m$

$$a_n = \frac{4V_{dc}}{n\pi} \sum_{k=1}^m \cos n\alpha_k \quad (7)$$

$$0 < \alpha_1 < \alpha_2 < \alpha_3 < \dots < \alpha_m < \frac{\pi}{2} \quad (8)$$

For any odd harmonics can be expressed up to  $k^{th}$  term, where m is the number of variable corresponding to switching angle  $\alpha_1$  through  $\alpha_m$  of the first quadrant

Total Harmonics Distortion (THD);

$$THD = \frac{1}{\text{fundamenta l}} \left[ \sum_{n=2}^{\infty} (n^{th} \text{harmonic components})^2 \right]^{1/2} \quad (9)$$

IV. INVERTER EFFICIENCY

The efficiency of a hybrid inverter is higher than a conventional inverter, for the applications where the switching losses are bigger. The efficiency of the proposed structure is between the efficiency of the ideal hybrid inverter and a conventional multilevel inverter fully supplied with dc-dc converters. At the same time, it is an attractive solution to get a large number of levels together with a good efficiency.

TABLE 2.

	Cascade	Hybrid	New Hybrid
No of level L S=No of stages S=3	2s+1 7 level	2 <sup>s+1</sup> -1 15 level	3 <sup>s</sup> 27 level
Input DC voltage	V <sub>dc</sub> 1 V <sub>dc</sub>	2 <sup>s-1</sup> V <sub>dc</sub> 4 V <sub>dc</sub>	3 <sup>s-1</sup> V <sub>dc</sub> 9 V <sub>dc</sub>

COMPARISON OF MULTILEVEL INVERTER

The comparison between cascaded, hybrid and new hybrid of multi level inverter as shown the table 2. Here the number of levels is higher than the other methods. For the reduced number of stages, the output and number of levels are high. The harmonic distortions are reduced in the proposed method and viewed in the result analysis.

V. SIMULATION RESULTS

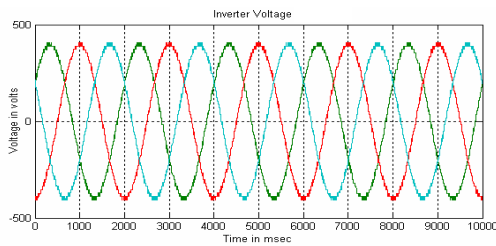


Figure 5. Three phase output Voltage of Multilevel Inverter

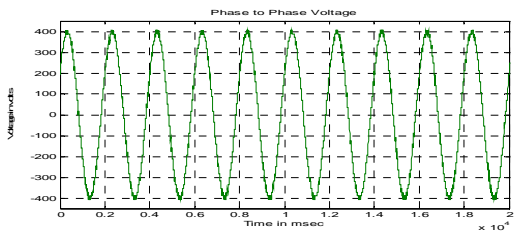


Figure 6. Line Voltage of Multilevel inverter

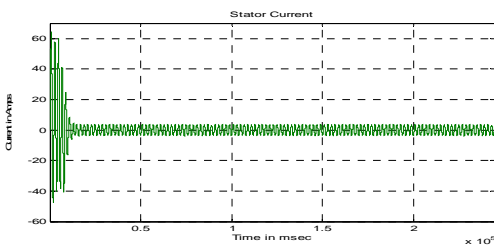


Figure 7. Stator current wave form of motor.

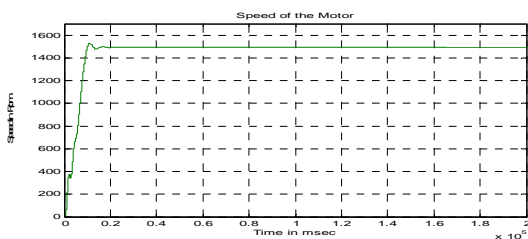


Figure 8. Speed of the motor.

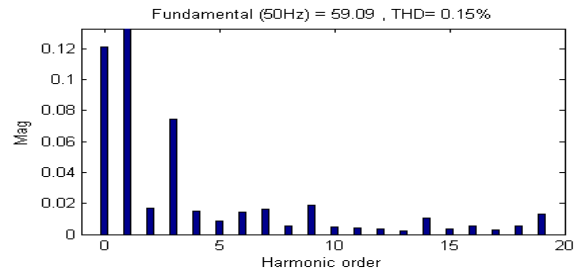


Figure 9. FFT harmonic spectrum output.

VI. RESULT ANALYSIS

The steady state three phase output voltage and line voltage are shown in the figure 5 and figure 6 respectively. The amplitude of the output voltages 400V, which is derived from the 27 level inverter. The output voltage of the inverter, which is fed as an input to the motor is nearly sinusoidal because the harmonics were reduced.

The stator current of the multilevel inverter fed induction motor is shown in figure 7. The speed of the motor is plotted in figure 8 for the proposed 27 level inverter. In a short duration of time, the rated speed of 1400 rpm is acquired. When the load is operated at the time of starting, the starting current is high up to maximum and during the occurring period, the current drops to minimum which is shown in figure 7.

As per the design of the proposed 27 level multilevel inverter, the total harmonic distortion is dramatically reduced to 0.15%. as shown in figure 9.

Thus from the results shown it is concluded that the output voltage is up to the required range which operate the load without any fluctuation, i.e. due to the reduction of lower order harmonics and good efficiency.

CONCLUSIONS

An improved new hybrid 27 level multilevel inverter structure is proposed. Basic new hybrid inverter scheme is to get the better sinusoidal output compared with low level inverters. The asymmetrical multilevel inverter is used to obtain a high resolution. By this method decrease the input voltage and get better efficiency in a 27 level multi level inverter structure. The asymmetrical hybrid technique is used to improve the level of inverter and extends the design flexibility and reduces the harmonics.

## APPENDIX.MOTOR PARAMETERS

Induction Motor Rating	3HP
Pole Pair	2
Stator Resistance	1.55 ohm
Rotor Resistance	1.25 ohm
Stator Leakage Inductance	0.172 H
Rotor Leakage Inductance	0.172 H
Mutual Inductance	0.166 H
Motor Inertia	0.016 Kg-m <sup>2</sup>

## REFERENCES

- [1] A. Nabae and H. Akagi. "A new neutral-point-clamped PWM Inverter", *IEEE Transactions on Industry Applications*, 17(5): 518–523, September 1981.
- [2] Y.S.Lai and et al. "Topology for hybrid multi level inverter", *IEE Proc-Electr.Power Appl.* Vol 149, No 6 nov 2002
- [3] T. Meynard and H. Foch. "Multi-level choppers for high voltage Applications", *EPE Journal*, 2(1):45–50, 1992.
- [4] O.M. Mueller and J.N. Park. Quasi-linear IGBT inverter topologies. *APEC'94 Conference Proceedings*, 1:253–259, Feb 1994.
- [5] M.D. Manjrekar, P.K. Steimer, and T.A. Lipo. "Hybrid multilevel power conversion system: A competitive solution for high power applications". *IEEE Transactions on Industry Applications*, 36(3): 834–841, May/June 2000.
- [6] K.A. Corzine, S.D. Sudhoff, and C.A. Whitcomb. "Performance characteristics of a cascaded two-level converter". *IEEE Transactions on Energy Conversion*, 14(3), September 1999.
- [7] A. Rufer, M. Veenstra, and K. Gopakumar. "Asymmetric multi level converter for high resolution voltage phasor generation", *EPE'99*.
- [8] P.K. Steimer and M.D. Manjrekar. Practical medium voltage inverter topologies for high power applications. *IAS'2001 Conference proceedings*, 3:1723–1730, September 2001.
- [9] M. Veenstra and A. Rufer. Control of a hybrid asymmetric multi-level inverter for competitive medium-voltage industrial drives. *IAS'2003*, 1:190 – 197, October 2003.
- [10] S. Mariethoz and A.C. Rufer. Design and control of asymmetrical multilevel inverters. *IECON'02*, November 2002.

## BIOGRAPHIES



**K. Ramani** was born in Vedaranyam on May 7, 1982. He is graduated in 2004 from Bharathiar University, Coimbatore and post graduated in 2006 at Anna University, Chennai. He is a Research scholar in Anna University Chennai under the guidance of Dr.A.Krishnan, Dean, K.S.Rangasamy College of Technology, Tiruchengode.. He is currently

working as a senior lecturer in the department of EEE at K.S.Rangasamy College of Technology, Tiruchengode from January 2006 onwards. He published 12 international/national conferences, journals. His research interests involve power electronics, inverter, modeling of induction motor and optimization techniques. He is guiding UG, PG Students. He is an ISTE, IETE member.



**Dr.A.Krishnan** received his PhD Degree in Electrical Engineering from IIT, Kanpur. He is a IEEE senior member. He is now working as a Dean at K.S.Rangasamy College of Technology, Tiruchengode and guide at Periyar University, Salem and Anna University, Chennai. His research interest includes Control System, Digital Filter, Power Electronics, Digital Signal Processing, and Artificial Intelligent

Techniques. He is a visiting professor in ISTE chapter and at foreign universities. He has been Published more than 250 technical papers at various National and International Conferences and Journals.