

Modeling of 11-Level Cascade Multilevel STATCOM

Jagdish Kumar¹, Biswarup Das², and Pramod Agarwal²

^{1,2} Indian Institute of Technology Roorkee, Roorkee, India

Emails: jk_bishnoi@yahoo.com,

biswafee@iitr.ernet.in, pramgfee@iitr.ernet.in

Abstract—This paper presents analytical approach for modeling of 11-level cascade multilevel STATCOM connected to power system for voltage regulation applications. A technique based on energy equivalence is proposed for computation of equivalent capacitance which represents true value of variable structure of capacitances connected in individual H-bridges. The necessity of equivalent capacitor is an essential requirement for accurate modeling and control system design for STATCOM.

Index Terms— cascade multilevel inverter, modulation index, static synchronous compensator, model order reduction, total harmonic distortion.

I. INTRODUCTION

Static Synchronous Compensator (STATCOM) is a power electronics based flexible alternating current transmission systems (FACTS) device extensively used for the purpose of reactive power compensation in the power systems. The main component of STATCOM is a voltage source inverter (VSI), which may be of multipulse or multilevel type. As compared to the hard-switched two-level pulse width modulation inverters, multilevel inverters offer several advantages such as their capabilities to operate at high voltage with lower dv/dt per switching, high efficiency, low electromagnetic interference etc [1]-[3]. Apart from being used in STATCOM, the multilevel inverters can provide important applications in distributed energy systems where ac voltage can be obtained by connecting dc sources such as batteries, fuel cells, solar cells, rectified wind turbines etc at input side of the inverters. The ac power thus obtained can be used directly for hybrid electric vehicles or may be interfaced to utility [2]-[4].

The multilevel inverters are further classified into (i) diode-clamped, (ii) flying capacitors, and (iii) cascade multilevel inverter (CMLI). Among these three, CMLI has a modular structure and requires least number of components as compared to other two topologies; as a result, it is widely used for above mentioned applications [4].

To analyze the dynamics of multilevel STATCOM, PSCAD/MATLAB type software are mostly used. The simulations with these programs are accurate but studies carried out are generally based on trial and error which requires much time and labor. Alternatively, control system design technique can be used, resulting in shorter design time with less effort. However, the application of

control system design technique requires a suitable and accurate system model.

Most of literatures [5]-[7] deal with the modeling of multipulse type inverter, where it is simple to develop an analytical model because structure of the multipulse inverter is fixed. But in case of multilevel inverters the structure is variable with time since dc sources are sequentially switched in and out of the current circuit. The major challenge in multilevel inverters modeling is how to represent this variable structure [8].

The present paper deals with the mathematical modeling of multilevel STATCOM, where, an equivalent value of dc sources (in general, capacitors) over one cycle period is computed using principle of energy equivalence. The mathematical model is developed using this equivalent capacitor value for analysis and control system design purpose.

II. MULTILEVEL STATCOM OPERATION

A. Basics

The multilevel STATCOM configuration consists of a voltage source inverter, dc side capacitors (C) with voltage v_{dc} on it, and a coupling reactor (L_c) or a transformer. The ac voltage difference across the coupling reactor produces reactive power exchange between the STATCOM and the power systems at the point of common coupling (PCC). If the output voltage of the STATCOM (v_c) is more than the system voltage (v_l), in that case, reactive power is supplied to the power system, while reactive power goes to STATCOM if v_c is less than that of v_l . To take effect of this bidirectional flow of reactive power, the STATCOM output voltage should be varied according to requirement of reactive power compensation, and this can be accomplished in two ways: i) by changing the switching angles while maintaining the dc capacitor voltage at a constant level (inverter type I control) or ii) keeping switching angles fixed and varying the dc capacitors voltages (inverter type II control) [5]. The variation of dc capacitors voltages is simply achieved by varying the active power transfer between STATCOM and power system by adjusting phase angle between v_c and v_l . Each of these control schemes has their own merits and demerits. In general, inverter type II control is preferred where very fast voltage control is not required such as in power system applications because THD injected can be minimized in this case [5]. In this work inverter type II

control scheme has been applied. The basic operating configuration of STATCOM is shown in Fig. 1.

B. Cascade Multilevel Inverter

The CMLI consists of a number of H-bridge inverter units with separate dc source for each unit and is connected in cascade or series as shown in Fig. 2. Each H-bridge can produce three different voltage levels: $+V_{dc}$, 0 , and $-V_{dc}$ by connecting the dc source to ac output side by different combinations of the four switches S_1 , S_2 , S_3 , and S_4 . The ac output of each H-bridge is connected in series such that the synthesized output voltage waveform is the sum of all of the individual H-bridges' outputs [2]-[4].

By connecting the sufficient number of H-bridges in cascade and using proper modulation scheme, a nearly sinusoidal output voltage waveform can be synthesized. The number of levels in the output phase voltage is given as $2s+1$, where s is the number of H-bridges used per phase. Fig. 3 shows an 11-level output phase voltage waveform using five H-bridges, where angles α_1 , α_2 , α_3 , α_4 , and α_5 are switching angles of H-bridges H_1 , H_2 , H_3 , H_4 , and H_5 respectively. The magnitude of the ac output phase voltage is given by $v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5}$ [3].

C. Switching Angles Selection

To synthesize multilevel ac output voltage using different levels of dc inputs, the semiconductor devices must be switched on and off in such a way that desired fundamental voltage obtained is nearly sinusoidal i.e. having minimum harmonic distortions. Different switching techniques are available for computing switching angles for the semiconductor devices [9]. For power system applications, generally fundamental frequency switching scheme is considered more suitable; in this scheme the devices are switched on and off once in every cycle, thereby producing less switching losses (more efficiency) [9]. Generally, the switching angles at fundamental frequency are computed by solving a set of nonlinear equations known as selective harmonic elimination (SHE) equations [3]-[4]. In SHE technique, in general, lower order harmonics are eliminated at the cost of generation of higher order harmonics, thereby increasing the total harmonic distortion (THD) in v_c . In the present work, an optimization technique is used for computation of switching angles which minimize THD due to all harmonic components up to 49th order; as a result, significant amount of THD reduction can be achieved as compared to SHE technique [10].

In general, the magnitude of voltage produced by 11-level CMLI is given by following relation [3]:

$$V_n = \sum_{n=1,3,5}^{\infty} \frac{4V_{dc}}{n\pi} (\cos(n\alpha_1) + \dots + \cos(n\alpha_5)) \quad (1)$$

From (1), the magnitude of fundamental voltage is as follows:

$$V_1 = \frac{4V_{dc}}{\pi} (\cos(\alpha_1) + \dots + \cos(\alpha_5)) \quad (2)$$

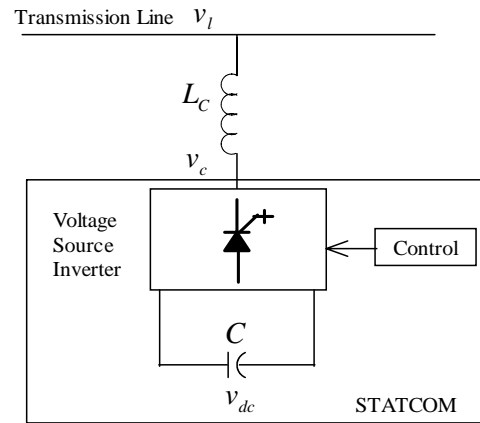


Fig. 1. Basic STATCOM configuration.

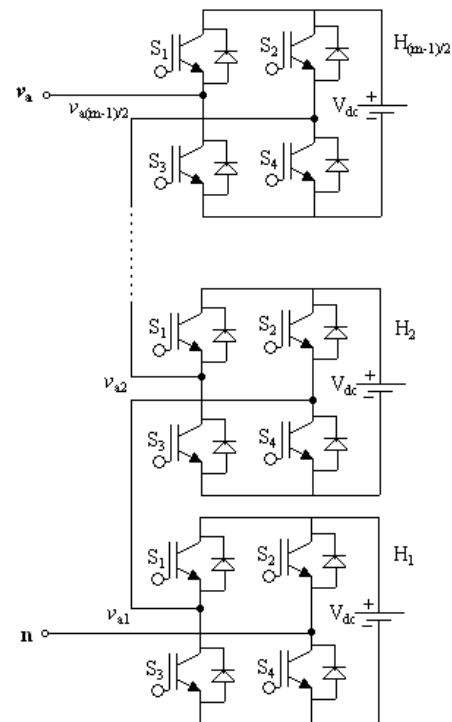


Fig. 2. Configuration of single-phase CMLI.

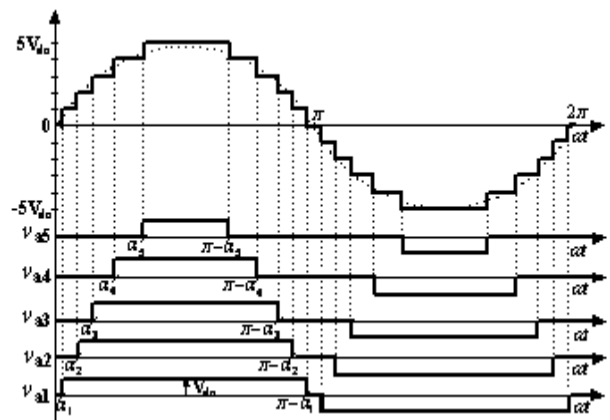


Fig. 3. Output voltage waveform of an 11-level CMLI at fundamental frequency switching.

Where n is the order of harmonic components and $\alpha_1 \dots \alpha_5$ are switching angles for five H-bridges such that $0 \leq \alpha_1 < \alpha_2 < \dots < \alpha_5 \leq \pi/2$. In three-phase power system,

triplen harmonic components are absent in line to line voltages, therefore, only non-triplen odd harmonic components of v_c are considered for THD optimization.

The objective function is formulated as follows:

$$\Phi(\alpha_1, \alpha_2, \alpha_3, \alpha_4, \alpha_5) = \sqrt{V_5^2 + V_7^2 + \dots + V_{49}^2} \quad (3)$$

The objective function (3) is minimized with equality constraints given by (2) and switching angles range $0 \leq \alpha_1 < \alpha_2 < \dots < \alpha_5 \leq \pi/2$ using MATLAB/Optimization Toolbox [11].

The switching angles and corresponding THD for the variation of modulation index (m) from 0 to 1 are calculated; the switching angles corresponding to minimum THD have been selected for the operation of CMLI. The minimum THD is obtained at $m = 0.9240$. The switching angles (in radians) and THD corresponding to this value of m are given in Table I. It is to be noted that modulation index (m) is defined as the ratio of ac output voltage obtained to the maximum obtainable ac output voltage [10].

TABLE I

m	α_1	α_2	α_3	α_4	α_5	THD
0.924	0.056	0.169	0.281	0.474	0.668	2.28%

III. MATHEMATICAL MODELING OF STATCOM

Single line diagram of a single generator feeding power to a load through transmission line is shown in Fig. 4(a). An inductive load is assumed to be connected at load bus. The load bus voltage may vary either due to variation in amount or nature of the load or it may vary due to supply side disturbances. In either case, it is required to keep the load voltage at desired level by generating/absorbing reactive power using STATCOM. For this purpose, a cascade multilevel STATCOM is connected at the load bus. As discussed in previous section, the amount of reactive power compensation is decided by the angle difference between load voltage and STATCOM output voltage, furthermore, the load voltage depends on the amount of reactive power compensation; therefore, a relation between this phase angle and load voltage is required to be established for proper and effective design of feedback control scheme. In following section this relation is established for the configuration shown in Fig. 4. Different symbols as used in Fig. 4(a) are as follows: R_S and L_S are resistance and inductance of transmission line; R_C and L_C are coupling reactor's resistance and inductance; active and reactive loads have been represented by R_L and L_L ; whereas, R_p represents switching losses. Various current and voltage variables are shown at appropriate place. In Fig. 4(b), d-q components of corresponding voltage and currents are shown.

In terms of instantaneous variables shown in Fig. 4, the ac-side circuit equation of STATCOM can be written as follows (calculations are carried out on per unit basis):

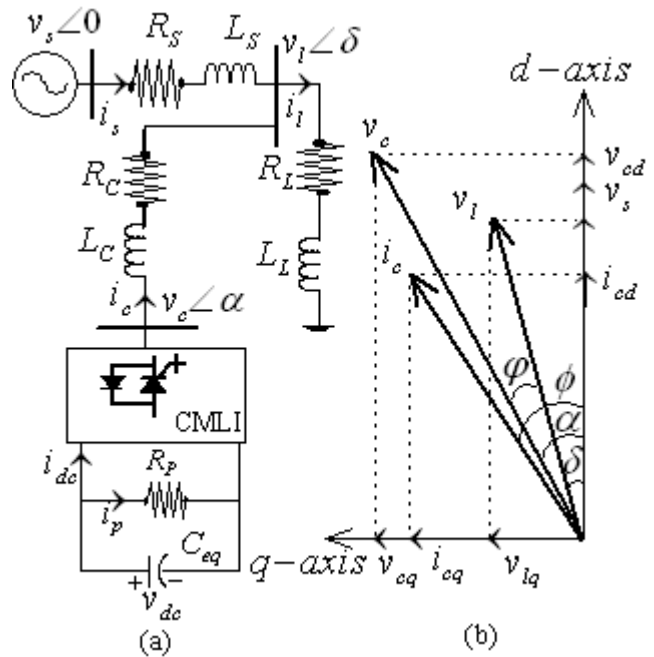


Fig. 4. (a) Multilevel STATCOM connected to power system (b) Phasor relation of d-q components of currents and voltages.

$$di_c / dt = -(\omega R_C / L_C) i_c + \omega(v_c - v_l) / L_C \quad (4)$$

Using the Park's transformation of variable as used in [5], equation (4) can be transformed into the synchronously rotating reference frame as follows:

$$\frac{d}{dt} \begin{bmatrix} i_{cd} \\ i_{cq} \end{bmatrix} = \omega \begin{bmatrix} -R_C / L_C & 1 \\ -1 & -R_C / L_C \end{bmatrix} \begin{bmatrix} i_{cd} \\ i_{cq} \end{bmatrix} + \frac{\omega}{L_C} \begin{bmatrix} v_{cd} - v_{ld} \\ v_{cq} - v_{lq} \end{bmatrix} \quad (5)$$

Where, ω is the speed of synchronously rotating reference frame in radians per second,

The d-q components of STATCOM voltage is given as $v_{cd} = kmv_{dc} \cos(\alpha)$, $v_{cq} = kmv_{dc} \sin(\alpha)$ (6)

Where m is modulation index, $k = \pi/4$ and v_{dc} is total capacitor voltage.

The dynamics of capacitor can be expressed as: $dv_{dc} / dt = -\omega C_{eq} (i_{dc} + v_{dc} / R_p)$ (7)

Neglecting switching and coupling reactor resistive losses, power at dc and ac sides of the inverter is equal, therefore, the capacitor current is given as:

$$i_{dc} = 3km(i_{cd} \cos(\alpha) + i_{cq} \sin(\alpha)) / 2 \quad (8)$$

Writing circuit equations for source and load variables in similar way as it has been written for STATCOM variables and applying transformation as applied in case of equation (4); load and source currents expression can be written as follows:

$$\frac{d}{dt} \begin{bmatrix} i_{ld} \\ i_{lq} \end{bmatrix} = \omega \begin{bmatrix} -R_L / L_L & 1 \\ -1 & -R_L / L_L \end{bmatrix} \begin{bmatrix} i_{ld} \\ i_{lq} \end{bmatrix} + \frac{\omega}{L_L} \begin{bmatrix} v_{ld} \\ v_{lq} \end{bmatrix} \quad (9)$$

$$\frac{d}{dt} \begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} = \omega \begin{bmatrix} -R_s & 1 \\ L_s & \\ -1 & -R_s \\ & L_s \end{bmatrix} \begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} + \frac{\omega}{L_s} \begin{bmatrix} v_s - v_{ld} \\ -v_{lq} \end{bmatrix} \quad (10)$$

Again from fig. 4(a), expression for load current can be written in terms of its d-q components as follows:

$$i_{ld} = i_{sd} + i_{cd}, \quad i_{lq} = i_{sq} + i_{cq} \quad (11)$$

Combining equations (5) - (11), following set of state-space equations is obtained:

$$\frac{d}{dt} \begin{bmatrix} i_{sd} \\ i_{sq} \\ i_{cd} \\ i_{cq} \\ v_{dc} \end{bmatrix} = \omega [A] \begin{bmatrix} i_{sd} \\ i_{sq} \\ i_{cd} \\ i_{cq} \\ v_{dc} \end{bmatrix} + \omega \begin{bmatrix} (L_L + L_C) \\ \sigma \\ 0 \\ -L_L \\ \sigma \\ 0 \\ 0 \end{bmatrix} v_s \quad (12)$$

$$A = \begin{bmatrix} -\sigma_1 & 1 & -\sigma_2 & 0 & -k_1 \cos(\varphi) \\ -1 & -\sigma_1 & 0 & -\sigma_2 & -k_1 \sin(\varphi) \\ -\sigma_3 & 0 & -\sigma_4 & 1 & k_2 \cos(\varphi) \\ 0 & -\sigma_3 & -1 & -\sigma_4 & k_2 \sin(\varphi) \\ 0 & 0 & -k_3 \cos(\varphi) & -k_3 \sin(\varphi) & C_{eq}/R_p \end{bmatrix}$$

Expression for load voltage can be obtained by eliminating derivative terms of source current in equation (10) with the help of relation given in equation (12), resulting expression of v_l in terms of its d-q components is:

$$v_l = \sqrt{v_{ld}^2 + v_{lq}^2}$$

$$v_{ld} = \beta_1 i_{sd} + \beta_2 i_{cd} + \beta_3 kmv_{dc} \cos(\varphi) + \beta_4 v_s$$

$$v_{lq} = \beta_1 i_{sq} + \beta_2 i_{cq} + \beta_3 kmv_{dc} \sin(\varphi) \quad (13)$$

Different notations used in equations (12) and (13) are related with system parameters in following way:

$$\sigma = (L_s L_L + L_s L_C + L_C L_L) / \sigma, \sigma_1 = (R_s L_L + R_s L_C + R_L L_C) / \sigma,$$

$$\sigma_2 = (R_L L_C - R_C L_L) / \sigma, \sigma_3 = (R_L L_s - R_s L_L) / \sigma,$$

$$\sigma_4 = (R_C L_s + R_L L_s + R_C L_L) / \sigma, \beta_1 = L_C (R_L L_s - R_s L_L) / \sigma,$$

$$\beta_2 = L_s (R_L L_C - R_C L_L) / \sigma, \beta_3 = L_s L_L / \sigma, \beta_4 = L_L L_C / \sigma,$$

$$k_1 = L_L km / \sigma, k_2 = (L_s + L_L) km / \sigma, k_3 = 3km / 2C_{eq},$$

$$\varphi = \alpha - \delta.$$

Equations (12) – (13) are nonlinear, if φ is regarded as input variable and v_l as output variable, in that case, a useful relation between these two variables can be obtained for small deviation about a chosen steady-state equilibrium point. This helps in deriving the transfer function between these two variables.

So far we have considered a single capacitor (C_{eq}) connected to CMLI at dc side (Fig. 4(a)), it has been assumed that the value of this single capacitor is equal to effective value of all capacitors connected to individual H-bridges in 3-legs. Now, in order to get an equivalent capacitor value to obtain appropriate transfer function for controller design a true value of C_{eq} is required.

Based on energy equivalence concept, equivalent capacitor is calculated as follows:

Considering half wave of Fig. 3, the first H-bridge conducts from α_1 to $\pi - \alpha_1$; it means capacitor C_1 remains in the circuit for a period of $\pi - 2\alpha_1$. Similarly, second H-bridge conducts from α_2 to $\pi - \alpha_2$ i.e. capacitor (C_2) remains in the circuit for a period of $\pi - 2\alpha_2$, proceeding in similar way the third, fourth and fifth capacitors conduct for $\pi - 2\alpha_3$, $\pi - 2\alpha_4$, and $\pi - 2\alpha_5$ period respectively. Let an equivalent capacitor for phase A be denoted by C_A with V voltage across it and it delivers same energy as delivered by these five capacitors in half cycle. This statement can be written mathematically as follows:

$$\frac{1}{2} \int_0^\pi C_A V^2 d(\omega t) = \frac{1}{2} \left(\sum_{i=1}^5 \int_{\alpha_i}^{\pi - \alpha_i} C_i v_i^2 d(\omega t) \right) \quad (14)$$

Here C_i and v_i represent capacitance and voltage across the capacitor in individual H-bridges of phase A leg.

In general, individual capacitor voltage needs to be well balanced in order to have less distortion in output ac voltage; therefore, a rotating switching scheme as described in [3] is used. In rotating switching scheme, the switching angles are rotated among all H-bridges of a leg turn by turn, therefore, all capacitors should have equal value i.e. $C_1 = C_2 = \dots = C_5 = C$ (let). Voltage on all capacitors needs to be equal and it would be equal to $V/5$.

Simplifying equation (14) gives an equivalent value of capacitor in phase A and it is given as

$$C_A = (C/25\pi)[5\pi - 2(\alpha_1 + \alpha_2 + \alpha_3 + \alpha_4 + \alpha_5)] \quad (15)$$

For three-phase configuration, three legs are connected in parallel and switching angles for each phase are equal (only these are displaced by $2\pi/3$), therefore, equivalent capacitor value (C_{eq}) over a cycle can be taken as three times to the equivalent value of each phase, i.e.

$$C_{eq} = (3C/25\pi)[5\pi - 2(\alpha_1 + \alpha_2 + \alpha_3 + \alpha_4 + \alpha_5)] \quad (16)$$

From relation (16), equivalent value of capacitor is computed at two extreme operating switching angles of CMLI: (i) when none of H-bridges conduct (producing zero output voltage) i.e. $\alpha_1 = \alpha_2 = \dots = \alpha_5 = \pi/2$, in this case $C_{eq} = 0$ (from equation (16)); (ii) when all H-bridges conduct simultaneously (producing maximum output voltage, corresponding to unity modulation index). The switching angles in this case are zero, i.e. $\alpha_1 = \alpha_2 = \dots = \alpha_5 = 0$, using equation (16) $C_{eq} = 3C/5$. These two extreme values of equivalent capacitor seem to be true because when all H-bridges conduct simultaneously, equivalent capacitor would be $3C/5$. Therefore, it validates the proposed procedure for equivalent capacitor calculation. Moreover, a similar relation has been used in [12] for five level CMLI validating the proposed procedure.

Linearizing equation (12)-(13) around particular steady-state operating point and linearized equations are as follows:

$$d\Delta X / dt = A_\Delta \Delta X + B_\Delta \Delta \varphi; \Delta v_l = C_\Delta \Delta X + D_\Delta \Delta \varphi$$

Where $\Delta X = [\Delta i_{sd} \ \Delta i_{sq} \ \Delta i_{cd} \ \Delta i_{cq} \ \Delta v_{dc}]^T$, A_Δ is equal to A at operating point, B_Δ , C_Δ , and D_Δ are given as:

$$B_{\Delta} = \omega \begin{bmatrix} k_1 v_{dc0} \sin(\varphi_0) \\ -k_1 v_{dc0} \cos(\varphi_0) \\ -k_2 v_{dc0} \sin(\varphi_0) \\ k_2 v_{dc0} \cos(\varphi_0) \\ k_3 (i_{cd0} \sin(\varphi_0) - i_{cq0} \cos(\varphi_0)) \end{bmatrix}$$

$$C_{\Delta} = \frac{1}{v_{l0}} \begin{bmatrix} \beta_1 v_{ld0} \\ \beta_1 v_{lq0} \\ \beta_2 v_{ld0} \\ \beta_2 v_{lq0} \\ \beta_3 k (v_{ld0} \cos(\varphi_0) + v_{lq0} \sin(\varphi_0)) \end{bmatrix}^T$$

$$D_{\Delta} = \frac{\beta_3 k v_{dc}}{v_{l0}} \left[(-v_{ld0} \sin(\varphi_0) + v_{lq0} \cos(\varphi_0)) \right] \quad (17)$$

State-variables variation as a function of load angle ($\Delta\varphi$) is plotted in Fig. 5 and these results are similar as obtained in [5] for multipulse inverter.

Corresponding steady-state values of variables and system parameters are given below (in pu):

$$i_{cd0} = -0.0, \quad i_{cq0} = -0.23, \quad v_{ld0} = 0.0, \quad v_{dc0} = 0.95,$$

$$v_{lq0} = -0.01, \quad \varphi_0 = -0.0103 \text{ rad}, \quad \omega = 314 \text{ rad/sec}$$

$$R_p = 78, \quad C_{eq} = 0.07, \quad R_s = 0.02, \quad L_s = 0.08,$$

$$R_c = 0.0, \quad L_c = 0.52, \quad R_L = 2, \quad L_L = 4.$$

The transfer function obtained from (17) relating Δv_l and $\Delta\varphi$ is of fifth order and it is reduced using model order reduction technique [11] to third order as given below.

$$\frac{\Delta v_l(s)}{\Delta\varphi(s)} = \frac{4.09s^2 + 730s - 62780}{s^3 + 261s^2 + 5048s + 27670} \quad (18)$$

Using transfer function given by (18), a PI controller is designed based on Ziegler-Nichols technique and corresponding step response of load voltage is shown in Fig. 6.

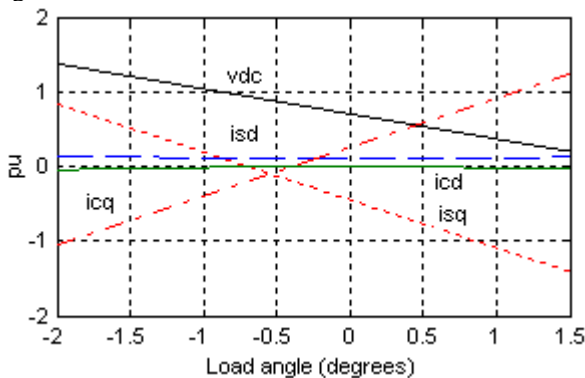


Fig. 5. Steady-state solutions.

IV. CONCLUSION

Mathematical modeling of a cascade multilevel inverter is carried out in this paper for transfer function derivation. More importantly, a concept of equivalent capacitor representing complete variable structure of CMLI is introduced. By taking into account the equivalent value of capacitor a transfer function relating

load bus voltage and load angle (phase angle between system load voltage and STATCOM output voltage) has been derived. The derived transfer function is very useful in control system design analysis.

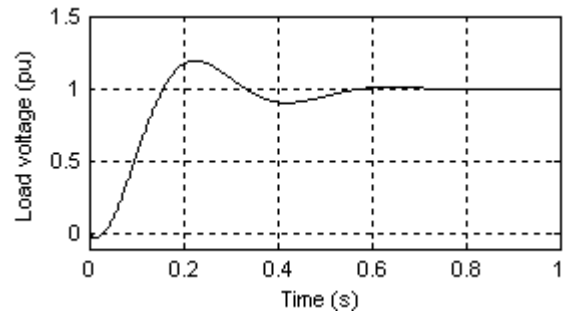


Fig. 6. Step response of load voltage.

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