

New Three-Input XOR and XNOR Gates Based on MOBILE and Application to a Full Adder

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Abstract— In this paper we propose new three-input XOR and three-input XNOR gate based on generalized threshold gate (GTG) topology. The GTG topology is main part is monostable-bistable logic element (MOBILE). The proposed gates use fewer elements count in comparison with other implementations which utilize MOBILE as a main structure. By exploiting the new three-input XOR gate and a carry generator, we present a full adder. All the circuits are simulated by using HSPICE simulator.

Index Terms_ monostable-bistable logic element, resonant tunneling diode, threshold gate, multi threshold threshold gate, generalized threshold gate.

I. INTRODUCTION

Resonant tunneling diodes (RTDs) have attracted much interest due to fast switching time, versatile functionality and unique negative resistance characteristics based on quantum transport phenomena. Compared to single electron transistors and more advanced quantum dot architectures, resonant tunneling devices are already operating at room temperature. Moreover, using RTDs in circuit design lead to a fewer element counts in comparison with the conventional designs such as CMOS etc. [1]. As shown in Fig. 1(a), RTD I-V characteristic exhibits a Negative Differential Resistance (NDR) behavior. The basic idea behind resonant tunneling device circuit design is to exploit this nonlinear I-V characteristic. Referring to the figure, for each current point there would be two corresponding stable voltages. Hence, if one considers the device a resistor, there would be two resistance states; the high resistance state and the low resistance state.

Most of the RTD based logic circuits include a MOBILE as their main part. The MOBILE consists of two RTDs in series at least, plus an edge triggered clock; V_{bias} (see Fig 1(b)). Its operation is based on switching of the two RTDs between the mentioned low and high resistance states [2].

When the bias voltage V_{bias} is in low logic state, both RTDs are in on state (low resistance state). By increasing the V_{bias} to an appropriate voltage called *switch voltage*, one of the RTDs which has the lowest peak current (the smallest area), is switched; i.e. changes its state from on state to off state. If the load RTD switches, the output logic will remain low and if the driver RTD switches, the

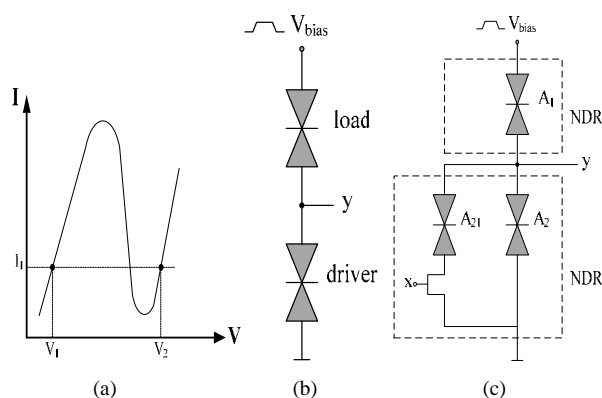


Figure. 1. (a) I-V characteristic of a typical RTD. For each constant current such as I_1 , there are two corresponding stable voltages i.e. V_1 and V_2 . An RTD in V_1 working point may be considered a low resistance (on state) and in V_2 working point, may be considered as high resistance (off state). (b) The simplest MOBILE architecture. When the clock, V_{bias} , increases from low state to its switch value, the RTD with the smallest area will be switched (quenched) and its state changes to off state while the other RTD will remain in on state. (c) a simple NOT gate based on MOBILE structure.

output will become high. Implementing MOBILE based logic gates, usually relies on changing the effective areas of RTDs by applying the logical inputs to some control transistors [3].

Fig. 1(c) shows a simple inverter based on MOBILE. . By applying logic 1 to the gate of the control transistor, the driver RTD area is added to A_{21} RTD, therefore, the load RTD quenches and the output logic will become low.

By applying 0 logic to the input, the effective area of the driver RTD will be less than the load RTD; consequently, the driver RTD switches and the output logic will become high [4].

Threshold Gate (TG), Multi Threshold Threshold Gate (MTTG) and Generalized Threshold Gate (GTG) are the three famous topologies for implementing logic functions based on MOBILE structure. The TG topology presented by C. Pacha *et. al.* in 2000. The MTTG topology that is an extension of TG, introduced by J.M. Quintana *et. al.* in 2003. The MTTG has more than one threshold; consequently has better functionality than TG. Moreover, this topology is a multi-output structure.

Another extension for TG is GTG topology which has introduced by M. Avedillo *et. al.* in 2005. This topology utilizes a combination of arithmetic functions and logic functions for implementing a logic gate; therefore it also has more functionality than TG. In this paper, we present a new three-input XOR gate and a new three-input XNOR gate based on GTG topology.

Some of the mentioned topologies presented two-input XOR and/or XNOR gates previously. In some of them there are some limitations for implementing two-input or three-input XOR and/or XNOR gates in the same topology.

In this paper a new three-input XOR and a new three-input XNOR gates which are based on GTG topology are presented. To the best of authors' knowledge, it is the first time that these gates are presented on GTG topology. The rest of this paper is organized as follows. In Section II, we present a briefly survey of the previous works. In Section III the new XOR and the XNOR gates are introduced and the simulation results are shown. The conclusions are drawn in Section IV.

II. A BREIF REVIEW OF PREVIOUS WORKS

A. Threshold Gate (TG)

TG topology is one of the MOBILE based technologies which is suitable for implementing threshold logic functions [4]. A TG structure is defined as a logic gate with n binary input variables; $x_i (i=1...n)$ and one binary output; y . There are also a set of n real numbers, corresponding to n inputs, called the weights; w_1, w_2, \dots, w_n , and another real number, called the threshold; T . Its input-output relationship is defined in (1).

$$y = \begin{cases} 1 & \text{if } \sum_{i=1}^n w_i x_i \geq T \\ 0 & \text{otherwise} \end{cases} \quad (1)$$

In the above relation, the sum and the product operations are the conventional mathematical operations, rather than the logical operations. The set of weights and the threshold is usually denoted in a more compact vector notation as $[w_1, w_2, \dots, w_n; T]$. A basic TG topology is shown in Fig. 2. In the figure, a two-input TG gate $[w_k, w_l; T]$ is depicted. w_k determines the weight for the first input which is a positive weight and w_l determines the weight for second input which is negative. The two parameters of A_1 and A_2 are determined by the desired threshold value to be implemented. The characteristics such as speed, power dissipation and robustness against technical variations are related to the A_n and A parameters and should be selected according to the utilized technology [7].

B. Multi Threshold Threshold Gate (MTTG)

The concept of TG can be extended to implement MTTG topology [5-7]. By connecting three or more

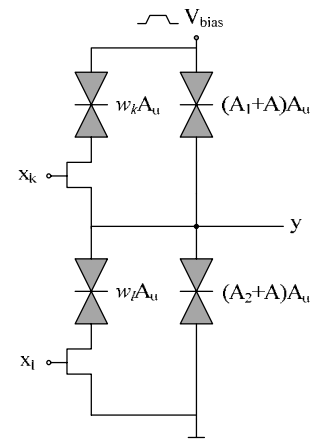


Figure 2. A basic TG topology (two-input).

RTDs in series, instead of two RTDs in TG, a conventional MTTG is formed. This structure is able to implement multi threshold logic functions.

In MTTG topology a boolean function; y , with the thresholds; $T_i (i=1, \dots, k)$, the weights; $w_1 \dots w_n$, ($w_j \in N^+$), and boolean inputs; $x_1 \dots x_n$, is defined as (2),

$$y = \begin{cases} 1 & \text{if } T_{2j-1} \leq \sum_{i=1}^n w_i x_i < T_{2j} \\ & \text{with } T_{j+1} > T_j (j = 1, 2, \dots, k/2) \\ 0 & \text{otherwise} \end{cases} \quad (2)$$

MTTG topology has two different versions, MTTG-1 and MTTG-2 [7]. Fig. 3 illustrates a two-input generic MTTG-1 topology. Different functions can be realized by adjusting the RTD areas to obtain the required current relationship among different NDRs, in both MTTG topologies. As reported in the literature, with three-series connected RTDs, 143 different three-input functions can be implemented using MTTG topologies which is 39 more functions than TG topology with two series-connected RTDs [4]; therefore MTTG has more functionality. The MTTG is also denoted by a vector such as $[w_1, w_2, \dots, w_n; T_1, \dots, T_k]$ that w_i can not be negative. Moreover, MTTG is able to produce two different outputs in a single structure i.e. MTTG is a multi output structure.

C. Generalized Threshold Gate (GTG)

Fig. 4 illustrates the GTG topology. By replacing the single control transistor in TG topology, with an arbitrary combination of series or parallel transistors, the GTG topology is realized [8,9]. This topology results in an easy technique for implementing complicated functions with fewer NDR devices. The input- output relationship for a generic GTG topology is shown in (3). Where T is the threshold, $w_{1i} (i=1, \dots, n)$ are positive weights, $w_{2j} (j=1, \dots, m)$ are negative weights, y is the output and $x_1 \dots x_k$ are the boolean inputs.

$$y = \text{sign}\{w_{11}f_1(x_1, \dots, x_k) \dots + w_{1n}f_n(x_1, \dots, x_k) - w_{21}g_1(x_1, \dots, x_k) \dots - w_{2m}g_m(x_1, \dots, x_k) - T\} \quad (3)$$

III. DESIGN NEW THREE_INPUT XOR AND XNOR GATES BASED ON GTG

XOR and XNOR gates could not be implemented in TG topology because implementing these functions requires two threshold values; however TG has only one threshold. Implementing two-input XNOR gate in the MTTG topology is also not possible [6,7] though two-input XOR is already presented in this topology [6,7]. In this way, three-input XOR gate in the MTTG topology is also not practical [7] however three-input XNOR was presented. Another two-input XOR based on MOBILE gate was introduced.

In this paper a new XOR gate and a new XNOR gate are introduced based on GTG topology. For achieving these XOR and XNOR functions, we assume that the proposed GTG structure [8], accepts different RTDs in terms of area.

Equation (4) shows the boolean function for three-input XOR gate and (5) shows the implementation of (4) by boolean operation plus threshold function for three-input XOR gate. Equation (5) is suitable for GTG implementation. In these two relations, \vee and \wedge are the boolean OR and AND functions respectively. The $-$ sign and $+$ sign are arithmetic subtraction and addition functions respectively. The “*sign*” is sign function which is equal to 1 if its arguments are greater than or equal to zero and is equal to 0 if its arguments are negative.

$$x_1 \oplus x_2 \oplus x_3 = (x_1 \wedge \bar{x}_2 \wedge \bar{x}_3) \vee (\bar{x}_1 \wedge x_2 \wedge \bar{x}_3) \vee (\bar{x}_1 \wedge \bar{x}_2 \wedge x_3) \vee (x_1 \wedge x_2 \wedge x_3) \quad (4)$$

$$y = \text{sign}\{[4(x_1 \wedge x_2 \wedge x_3) + 2(x_1 \vee x_2 \vee x_3)] - 2[(x_1 \wedge x_2) \vee (x_1 \wedge x_3) \vee (x_2 \wedge x_3)] - 1\} \quad (5)$$

Fig. 5 depicts the proposed three-input XOR gate based on GTG structure. The NDR_0 implements the positive terms; $[4(x_1 \wedge x_2 \wedge x_3) + 2(x_1 \vee x_2 \vee x_3)]$, and NDR_1 implements the negative term; $-2[(x_1 \wedge x_2) \vee (x_1 \wedge x_3) \vee (x_2 \wedge x_3)]$. However, w_2 is for adjusting the threshold value. For achieving XOR function the threshold value is set to 1.

Equation (6) shows the boolean function for three-input XNOR gate and (7) shows the implementation of (6) by boolean operation plus threshold function for three-input XNOR gate

$$x_1 \otimes x_2 \otimes x_3 = (\bar{x}_1 \wedge \bar{x}_2 \wedge \bar{x}_3) \vee (\bar{x}_1 \wedge x_2 \wedge x_3) \vee (x_1 \wedge \bar{x}_2 \wedge x_3) \vee (x_1 \wedge x_2 \wedge \bar{x}_3) \quad (6)$$

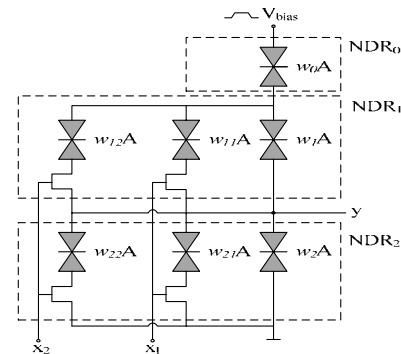


Figure 3. A two-input MTTG-1 topology.

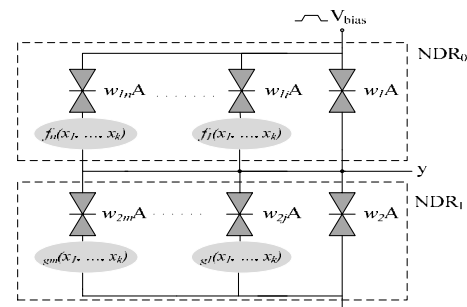


Figure 4. A generic GTG topology.

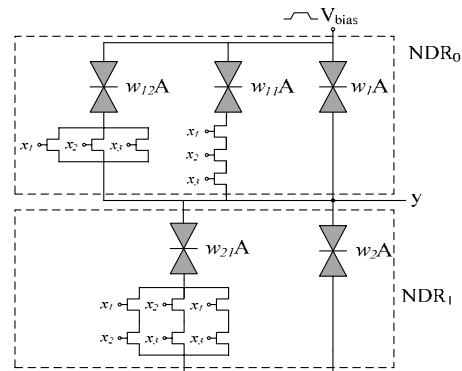


Figure 5. The proposed XOR gate circuit that uses GTG topology. The characteristics are as follows: $A=0.1\mu\text{m}^2$, $w_1=10$, $w_{11}=4$, $w_{12}=2$, $w_2=11$, $w_{21}=2$, also $V_{\text{bias}}=0.8\text{V}$.

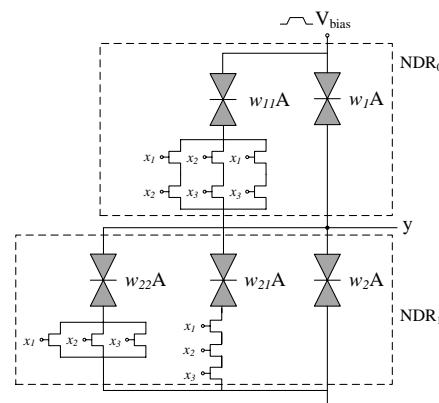


Figure 6. The proposed XNOR gate circuit that uses GTG topology. This function uses negative threshold value for correct operation. The design characteristics are as follows: $A=0.1\mu\text{m}^2$, $w_1=11$, $w_{11}=2$, $w_2=10$, $w_{21}=4$, $w_{22}=2$ and $V_{\text{bias}}=0.8\text{V}$.

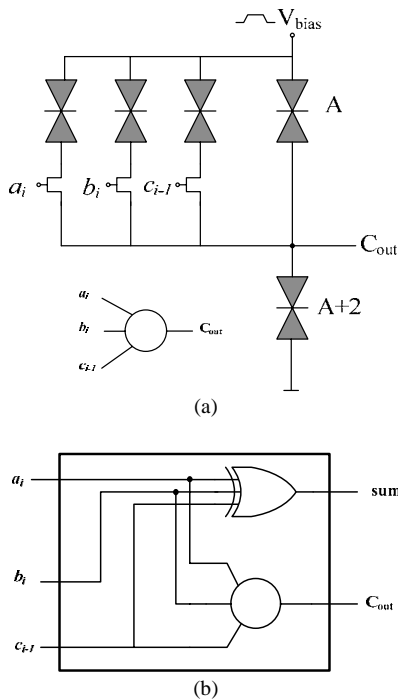


Figure 7. (a) The carry generator circuit [1]. (b) a full adder comprises a three-input XOR gate and a carry generator.

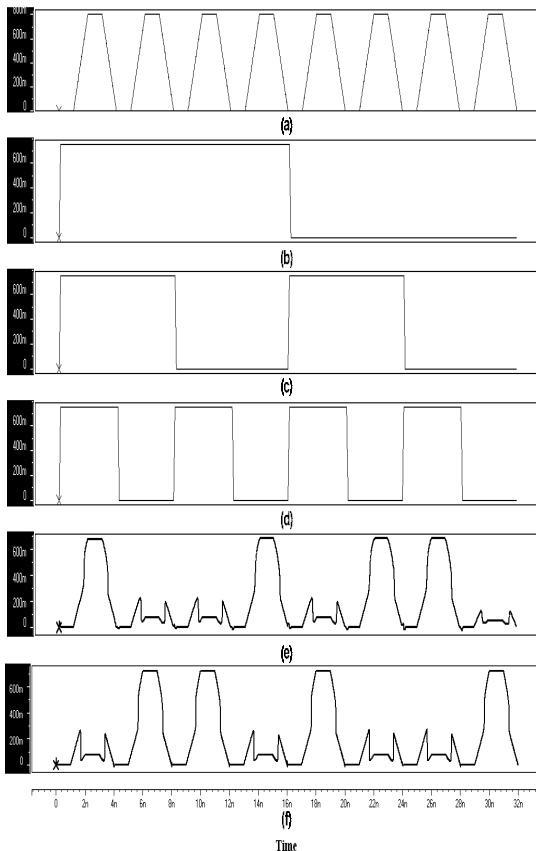


Figure 8. (a) The clock which is applied to the MOBILE. (b), (c) and (d) are input waveforms which produce eight different transitions. (e) the output of the three-input XOR gate circuit and (f) the output of the three-input XNOR gate circuit. (g) the carry output.

$$y = sign\{-4(x_1 \wedge x_2 \wedge x_3) - 2(x_1 \vee x_2 \vee x_3)\} + 2[(x_1 \wedge x_2) \vee (x_1 \wedge x_3) \vee (x_2 \wedge x_3)] + 1 \quad (7)$$

Fig. 6 illustrates the proposed three-input XNOR gate based on GTG structure. The NDR_0 implements the positive term, $2[(x_1 \wedge x_2) \vee (x_1 \wedge x_3) \vee (x_2 \wedge x_3)]$, and NDR_1 implements the negative terms, $[-4(x_1 \wedge x_2 \wedge x_3) - 2(x_1 \vee x_2 \vee x_3)]$. As shown in the figure, w_2 is for adjusting the threshold value which is a negative value for achieving XNOR function the threshold value is set to -1.

The carry generator circuit is introduced by C. Pacha [4], see Fig. 7 (a). This carry generator produces C_{out} in a single stage. We utilize the advantage of introduced carry generator to implement a full adder. Fig. 7 (b) shows a block of a full adder that comprises a three-input XOR gate and a carry generator. The carry generator circuit along with our proposed three-input XOR gate is able to implement a high performance full adder because it has not a long critical path, i.e. the full adder generates sum and $carry$ in a single stage.

Fig. 8 (a) shows the clock signal; V_{bias} , which is applied to the circuits. Fig. 8 (b), (c) and (d) depict eight different sets of three inputs that are applied to the XOR and the XNOR gates sequentially and the HSPICE simulation results for these gates are depicted in Fig. 8 (e) and (f) respectively.

For achieving the (5) and (7) and designing new XOR and XNOR gates, we add some features to standard GTG topology as follows:

- For the first time, we use a negative threshold in GTG based circuit design in order to obtain XNOR function.
- In standard GTG [8], all RTDs have the same weights; though we use different weights for different RTDs to obtain XOR and XNOR circuits.

In comparison with other three-input XOR gates that consist of cascading two, two-input XOR [4,5], the proposed XOR has a more simple design and fewer element counts. For example, the previous designs use two clocks for producing the output but our design requires only one clock signal. Also our XNOR has simpler design and fewer devices in compare with XNOR proposed in [5].

Our proposed circuits are the first MOBILE based designs that implement three-input XOR circuits in a single structure, i.e. a single gate in transistor level. Implementing XOR function in single structure (single block) enables designers to design more efficient full adders in comparison with the previous full adders that are based on cascading of two two-input XOR gates [4,5] to achieve a three-input XOR gate.

IV. CONCLUSION

In this paper, to the best of authors' knowledge, a new three-input XOR gate circuit and a new three-input XNOR gate circuit based on generalized threshold gate (GTG) are introduced for the first time. The GTG topology uses MOBILE as its main part. Moreover, we present a full adder that is comprises our new XOR gate and a carry generator. A simulation for all combination of inputs is done and the results are drawn.

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