

Synthesis of Low Power Sequential Circuit

BALJIT KAUR

Deptt. of Electronics and communication Engineering

National Institute Of Technology, Kurukshetra

E-mail: baljitaries@gmail.comwww.nitkkr.ac.in

Abstract:- Low power design is most required now a days due to scaling down the technology where minimizing the voltage level is the most effective way to minimize the power consumption. This paper presents a double pulse flip flop implemented using 0.18 μm technology. The proposed flip flop avoids unnecessary switching and stacking of transistors and thus consume less power as compared to conventional flip flops. A pulse generator is used to generate less width pulses, which will be helpful in increasing the clock frequency. A low power sequential circuit is designed and simulated using Mentor Graphics tools.

Key Words: - Double pulsed flip flop, Low power, High performance, VLSI.

I. INTRODUCTION

Flip-flops are critical timing elements in digital circuits and have a large effect on speed and power consumption of the digital circuits. One of the sources of the power consumption in digital systems is the clock tree which may consume up to 45% of the total system power. Therefore, the reduction in the clock tree power consumption may leads to a quantitative reduction in the system power consumption. We can see that, extensive research has been performed to develop fast and low-power flip-flops. For describing the performance of a flip-flop, primary measure is the minimum D-to-Q delay, as this determines how much time the flip flop takes to transfer the input at the output in other words it determines the impact on cycle time. The power consumption of circuits and systems is important in modern VLSI technology especially for low power applications and because of the continuous and fast increase in clock frequency and chip complexity. Hence the design of low power logic is one of the most important tasks to minimize the power consumption of digital circuits. Recently, pulsed latch structures have emerged as the fastest and power efficient flip-flop structures. So, because of their performance these double pulsed structures have been used in several commercial high performance micro-processors. The pulses are generated using pulse generator. This pulse generator can consume considerable energy. Therefore to avoid this pulse distortion pulses must be generated locally. Here we proposed a new flip-flop structure, the double-pulsed low power flip-flop (DFF), which has lowest-power consumption as compared to other conventional and other double pulsed flip-flops like double pulsed set conditionally reset flip flop (dpscrff). We have implemented this low power flip flop in the design of shift register to obtain the better performance from the system. In serial operation as shift register, it allows the higher frequency. As flip flops are the timing elements therefore to satisfy the timing constraints at the clock registers the various timing data (setup time, hold time and propagation delay) are described. We shall say that the data is

successfully stored within a register if the following timing constraints between the input data signal and the clock signal are satisfied.

Setup time:

It is defined as the minimum time such that the value of the data signal should be valid before the arrival of a clock signal.

Hold time:

It specifies the minimum time that the data signal should remain at a constant value after data storage is enabled.

Propagation delay:

It is defined as the delay between a latching event of the clock signal and the time of latched data is available at the output.

Since the importance of designing low-power and high performance timing elements has been recognized, therefore many latches and flip-flops have been designed. One of the latest low power flip flop is double pulsed set conditionally reset Flip-Flop (DPSCRFF) is a fastest. known flip-flop, but it consumes large amount of power due to redundant transition of internal nodes. In this paper we have proposed a simple double pulsed low power flip flop (DFF) structure, which have a small transparency window. This proposed structure avoids unnecessary internal node transitions to reduce power consumption as compared to DPSCRFF.

II. PROPOSED LOW POWER FLIP FLOP

In design of double pulsed low power flip-flop, pulse generator is modified, and the Latch part also modified to eliminates undesired glitch and extra dynamic power. Fig. 2 shows the design of the double pulsed low power flip-flop (DFF). It consists of a static latch and pulse generator. Static latch required two pulses p1 and p2, which are generated from the active clock edge, one pulse from the output of nand gate and another is obtained by passing the output of nand gate through a single inverter. Here in this proposed flip flop the second pulse is obtained by passing the output of nand gate through a single inverter instead of passing the pulse through three inverters in case of DPSCRFF. Therefore this proposed flip flop saves extra power dissipation.

When data D is 0 MP3 is on and MN3 is off, the pulse p1 will be low for small amount of time with in that time output node will be charged. When the input data D is '1' MP3 is off and MN3 is on pulse p2 will be high for small time and with in that time output node will be discharged. In pulse generator of DFF two invertors are

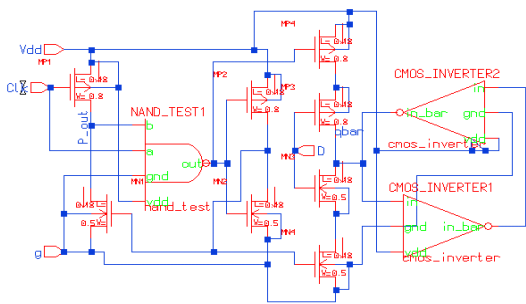


Fig.1: - Double Pulsed Low Power Flip Flop design

removed after NAND gate. NMOS is switched on early than DPSCRFF, because it is switched on after one inverter delay. By this way the width of pulses p1 and p2 is reduced, which reduces the transparency window of latch, which is desired for fast operation and low power applications. We can see the waveform of proposed circuit from fig. 2.

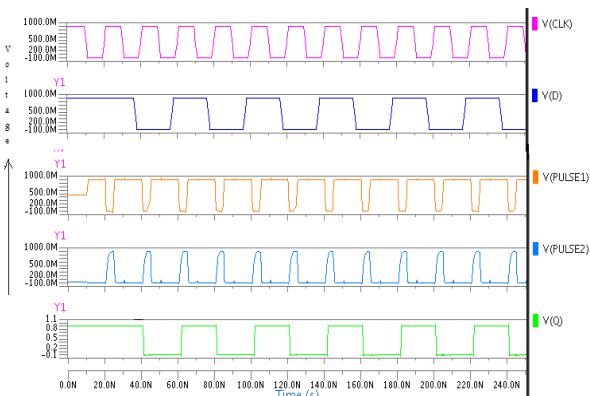
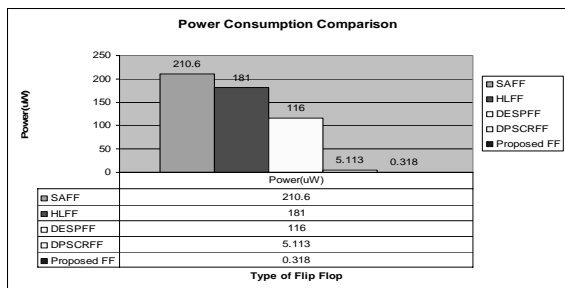


Fig.2 Waveform of Low Power Flip Flop

III. SIMULATION RESULTS

We have simulated the proposed DFF using mentor graphics tools. We found that the proposed low power flip-flop (DFF) has the power dissipation in approximately 300 nW while the conventional D flip flop and DPSCRFF [8] [9][10] has a power dissipation in hundreds of μW. We can see the comparison of different flip flop through this graph.



So it is our big achievement in the favour of low power digital circuit design. These result shows that DFF performance is better than DPSCRFF in terms of power dissipation in all situations. The static power reduction is obvious when clock and data are set to zero. The static power saving is considerable and considering the fact that many flip-flops are used in circuit over all power saving will be large for nanometer.

CONCLUSION

In this paper we have proposed new design of flip-flop, double pulsed low power flip flop (DFF). DFF eliminates unnecessary glitches, which consume more power. DFF consume less power for same delay as compared with DPSCRFF, which is one of the fastest known flip-flops. In serial operation as shift register DFF allows the higher frequency. The stacking of transistor in latch stage reduces sub-threshold leakage current and thus the static Power consumption is also less for DFF. This is better suited for low power circuits at deep submicron technology where leakages are more dominant.

REFERENCES

- [1] H. Partovi et al., "Flow-through latch and edge-triggered flip-flop hybrid elements," Digest ISSCC, February 1996.
- [2] F. Klass, "Semi-dynamic and dynamic flip-flops with embedded logic," in Symp. VLSI Circuits Dig. Tech. Papers, 1998, June.
- [3] "A new family of semidynamic and dynamic flip-flops with embedded logic for high-performance processors," IEEE J. Solid-State Circuits, vol. 34, May 1999.
- [4] W. C. Madden and W. J. Bowhill, "High input impedance strobed CMOS differential sense amplifier," U.S., Mar. 1990.
- [5] Albert Ma and Krste Asanovic, "A Double-Pulsed Set conditional Reset Flip-Flop", MIT LCS Technical Report, MIT-LCS-TR-844, May 2002.
- [6] T. Kobayashi et al., "A current-controlled latch sense amplifier and a static power-saving input buffer for low-power architecture," IEEE J. Solid-State Circuits, vol. 28, pp. 523–527, Apr. 1993.
- [7] V. Stojanović and V. Oklobdžija, "Comparative analysis of master-slave latches and flip-flops for high-performance and low-power systems," IEEE Journal Solid-State Circuits, vol. 34, no. 4, pp. 536–548, April 1999.
- [8] F. Klass et al., "A new family of semi-dynamic and dynamic flip-flops with embedded logic for high-performance procesors," IEEE JSSC, vol. 34, no. 5, pp.712–, May 1999.
- [9].Aliakbar Ghadiri, Hamid Mahmoodi, "Dual-Edge Triggered Static Pulsed FlipFlops" procee-dings of the 18th International Conference on VLSI Design on Embedded Systems Design (VLSID'05) pp 1063-9667, 2005.
- [10].Nedovic,N.;Oklobdzija, V.G.;Hybrid latch flip-flop with improved power efficiency Integrated Circuits and Systems Design, 2000. 18-24 Page(s):211 – 215, Sept. 2000.