FPGA implementation of Entropy based spectrum sensing technique for Cognitive Radio

Samrat L Sabat[1], Kishore Dapatri[1], and Siba K Udgata[2]
[1] School of Physics, University of Hyderabad, Hyderabad-500046,India
Email:slssp@uohyd.ernet.in
[2] Department of Computer & Information Sciences , University of Hyderabad, Hyderabad-500046,India
Email: udgatacs@uohyd.ernet.in

***Abstract*—This paper presents an architecture for FPGA implementation of entropy based spectrum sensing technique for detecting presence of signal in cognitive radio network (CRN) environment. Look-Up-Table (LUT) technique is used for computing entropy and log-likelihood ratio of entropy in Xilinx xtremeDSP development board. FPGA implementation of log-likelihood entropy-based spectrum sensing technique is validated with BPSK,QPSK and GMSK primary user signals in GSM 900 MHz band with Rayleigh and Rician multipath fading, for sample size 16, 32 and 64. Hardware in Loop (HIL) simulation is used for validating the implementation result with MATLAB simulation results. The hardware software co-simulation shows the matching of results between MATLAB and FPGA output. The algorithm works in the FPGA at operating frequency between 10 - 17MHz for GMSK, BPSK and QPSK signal of sample size 16, 32 and 64 respectively.**

***Index Terms*— Cognitive Radio (CR), FPGA, Spectrum Sensing, Hardware Software Co-Simulation**

I. INTRODUCTION

The need for new wireless and mobile technologies [1] are being continually driven by the potential demand for high data transfer rate and different bandwidth intensive multimedia applications. The spectrum scarcity for these new applications pose a big challenge for the researchers in academia and industry [2]. However, recent reports of FCC (Federal Communication Commission) reveals inefficient spectrum usage in spatial and temporal domain. Cognitive radios (CR) have emerged as a potential solution to handle spectrum scarcity problem. It allows unlicensed radio users to operate in licensed spectrum within tolerable range of interference level. This refers to dynamic spectrum access technique [3]. In CR, spectrum sensing plays a major functional role to detect the presence of primary signals [4].

For the spectrum sensing, mainly, three signal processing techniques such as (1) Energy detection [5], (2) matched filter based detection [6] and (3) cyclostationary feature detection [7] are proposed. Each detection technique has been refined to suit the requirement of CR. At very low signal to noise ratio (SNR) both energy detection and matched filter technique suffers from noise uncertainty. Cyclostationay technique requires high computational cost. Recently Entropy based spectrum sensing technique is studied and proposed to be an effective test method to increase the detection performance of matched filter in CR network [8]. The implementation of this test technique involves more computational cost.

In recent past FPGAs are being used for implementing computational intensive signal processing algorithms for different applications. In this paper, we implemented entropy-based spectrum sensing technique in Xilinx xtremeDSP development board that uses Virtex4-XCVSX35-10FFG668 FPGA. We have considered most similar conditions for the implementation as in [8]. We used general modulated signal such as BPSK, QPSK and GMSK signal in GSM 900MHz frequency band for realistic implementation with known signaling rate and carrier frequency but unknown noise and interference as primary user signal.

Rest of the paper is organized as follows: Section 2 discusses the entropy based spectrum sensing technique. Section 3 presents detailed architecture of the proposed implementation model. Simulation results and implementation issues are discussed in Section 4 followed by conclusions in Section 5.

II. ENTROPY BASED SPECTRUM SENSING ALGORITHM

The received modulated signal is embedded with white gaussian noise and multipath fading. This signal is fed to matched filter to maximize SNR. The matched filter output is considered to have N samples $\underline{x} = [x_1, x_2, .. x_N]$

The entropy of this signal e($\underline{x}$) can be estimated as in [8]

$$e(\underline{x}) = \sum_{k=1}^{L} -\left(\frac{n_k}{N}\right) \cdot \log_2\left(\frac{n_k}{N}\right) \quad (1)$$

where, n_k is number of samples with-in the K^{th} bin having $\left(l_k, l_{k+1}\right)$ as bin boundaries when the $\underline{x}$ is divided into L bins. The log-likelihood ratio of entropy can be estimated

$$\log\left(\frac{p(n_1,.......n_L \mid a_1)}{p(n_1,.......n_L \mid a_0)}\right) = \sum_{k=1}^{L} n_k .log\left(\frac{p_k(a_1)}{p_k(a_0)}\right) \quad (2)$$

$$= \sum_{k=1}^{L} \frac{n_k}{N} log\left(\frac{\frac{n_k}{N}}{p_k(a_0)}\right) - \sum_{k=1}^{L} \frac{n_k}{N} log\left(\frac{\frac{n_k}{N}}{p_k(a_1)}\right) \quad (3)$$

corresponding author: Samrat L Sabat, Email:slssp@uohyd.ernet.in

where, a_1=SNR > 0 and a_0=0.

$p_k(a)$ is the probability that a sample x_i falls within the k^{th} quantization interval (l_k, l_{k+1}), under the condition that $A = a$.

The detector output $\hat{\phi}(\underline{x})$ is the indicating function for primary user status and is given by

$$\hat{\phi}(\underline{x}) = \begin{cases} 1, & e(\underline{x}) < T \\ 0, & e(\underline{x}) \geq T \end{cases} \quad (4)$$

Where, T is the threshold computed as

$$T = m_0 + \sigma_0 Q^{-1}(1-\beta) \quad (5)$$

where m_0 and σ_0 are the mean and standard deviation of the signal when the primary user is idle (i.e., only noise is present). The m and σ of the input signal x can be calculated as

$$m_x = \sum_{i=1}^{N} x_i / N \quad (6)$$

$$\sigma_x = \sqrt{\sum_{i=1}^{N} x_i^2 / N} \quad (7)$$

III. FPGA IMPLEMENTATION

The architecture for implementing the algorithm for spectrum sensing is given in Fig. 1. The entropy and log likelihood ratio are calculated as in Eqn.(1) and Eqn.(3) respectively. The model is implemented in fading environment. The spectrum sensing architecture in Fig.1 comprises of 4 major blocks namely Entropy, Threshold, Decision logic and hardware co-simulation. The matched filter output signal is fed as input of entropy block to calculate the entropy of signal using Eqn.(1). The computation of entropy uses LUT approach for implementing in FPGA. The advantages of using LUT technique for entropy calculation is to reduce the computational burden and hardware resources in FPGA. In the decision logic block, the calculated entropy is compared with a threshold value for identifying the presence of signal as Eqn (4). In this paper, log-likelihood of entropy is also implemented for identifying the presence of signal together with normal entropy.

The architecture for computing entropy is given in Fig.2. This architecture consists of six subsystem blocks namely (1) Mean and Sigma (square root of power) computation block (2) Chebyeshev inequality test block (3) Histogram analysis block (4) Normal Entropy computation block (5) Probability block and (6) Log-likelihood entropy computation block. This gives estimated entropy value and log-likelihood ratio of entropy value for an applied modulated signal after matched filtering and sampling. Histogram block gets output from chebyeshev inequality test block for deciding design parameters K, and it does bin-adjustment for dividing the range of samples into L no. of bins with pre-calculated bin centers. Mean, Sigma computation block calculates the mean and square root of power as in Eqn. (6,7) using carry-look-ahead adder. Histogram block checks whether sum of total number of samples within K^{th} bin for *K=1* to *L* is equal to *N* or not, where N is the total number of samples in input signal. We have implemented and tested the entropy based spectrum sensing by using Hardware In Loop verification (HIL) technique. The HIL model of spectrum sensing is as shown in Fig. 1. HIL simulation is carried out in Xilinx System generator 10.1 environment. The computation of entropy and log-likelihood ratio involves computing logarithmic values for *N* number of times. Similarly, for computing sigma and probability of a sample within a particular bin requires computation of $(M\ X\ N)$ square root, where *M* is modulation alphabet and *N* is total number of samples taken for entropy processing. In our architecture, LUT approach is used to optimize the number of hardware resources and latency of the design. We have simulated, implemented and tested the architecture in FPGA for sensing the spectrum of BPSK, QPSK and GMSK modulations in GSM 900 MHz band. The simulated signals are generated by considering bandwidth as 200KHz, guard band as 100 KHz, sampling frequency as 100MHz and β=0.999 [8]. We have also considered Rayleigh fading channel & Rician fading channel effect to the signal. The fading parameters in the simulation are Doppler shift (f_d) = 300 Hz, Path delay (τ) = 0 - $1.e(-6)$ sec and Bit rate = 10 Kbps.

The simulation and implementation of the algorithm is carried out for signals of length *N*=16, 32, and 64. For the purpose of performance evaluation, estimated entropy values are computed using MATLAB . The hardware implementation of the algorithm is carried out using Xilinx system generator for DSP tool and Xilinx Virtex 4 XC4VSX35 (FFG668-10) device. The algorithm is validated for SNR range between 0 to 20dB in the steps of 1 dB. We compared MATLAB and FPGA output for computing log likelihood ratio of entropy for BPSK, QPSK and GMSK signal with different sample length as given in Fig.3-5 respectively. These figures reveal that results of FPGA implementation are almost matching with the MATLAB simulation results. The different kinds of resources required for computing normal entropy along with log-likelihood ratio entropy, and maximum operating frequency for BPSK, QPSK and GMSK are listed in Table I . The numerical accuracy of MATLAB simulation and FPGA output are tabulated in Table II for BPSK, QPSK and GMSK signals. These tables represent root mean square error between MATLAB and FPGA output. The difference between these two output values are due to the considered tradeoff between bit length and hardware resources.

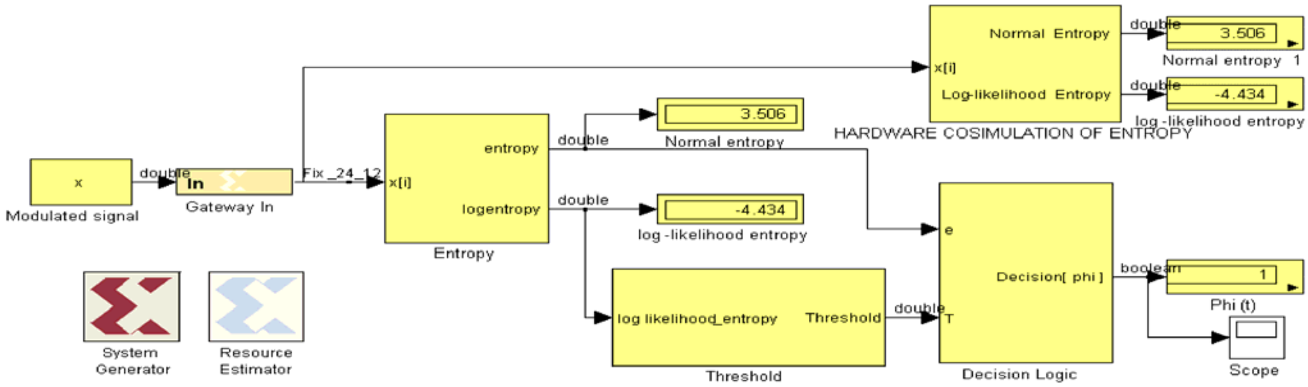

Figure 1. Spectrum sensing architecture for FPGA implementation

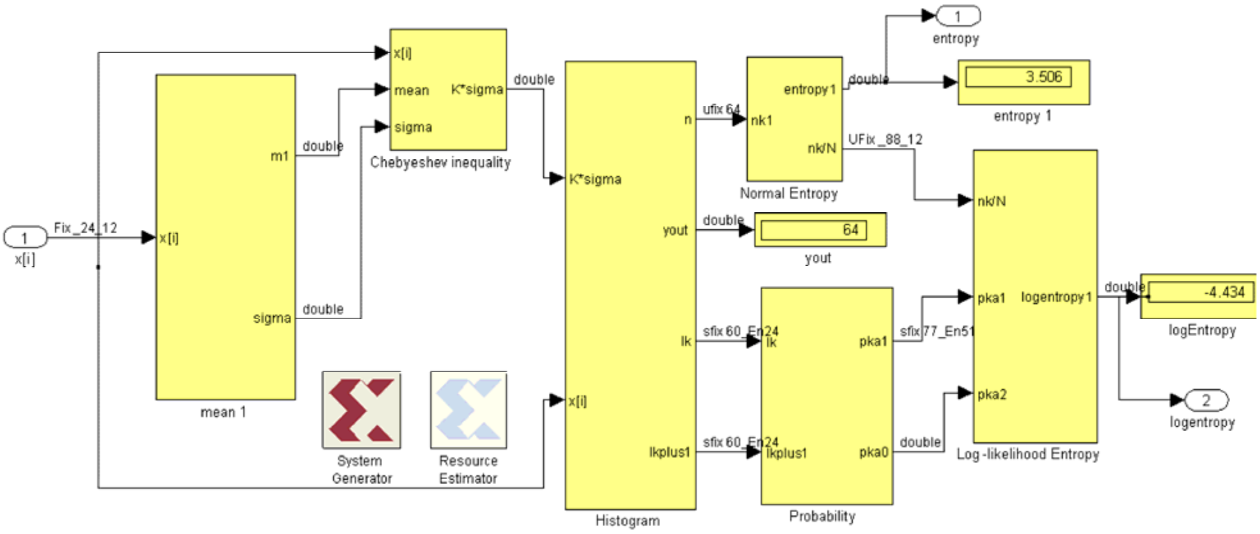

Figure 2. Entropy computation architecture for FPGA implementation

Table I

RESOURCE ALLOCATION AND MAXIMUM FREQUENCY OF ENTROPY BLOCK FOR BPSK, QPSK AND GMSK SIGNAL (DEVICE: VERTEX4 (XC4VSX35 - 10FFG668 - 10))

Modulation	No. of samples (N)	Slices	Slice Flip Flops	LUTS	DSP48s	Maximum Frequency (MHz)
BPSK	16	5896	1833	10211	110	15.515
BPSK	32	7546	1822	14153	175	14.486
BPSK	64	14850	1883	30720	179	9.978
QPSK	16	6437	1831	11060	130	15.204
QPSK	32	8088	1829	15132	186	14.173
QPSK	64	15358	1892	30720	190	9.675
GMSK	16	3673	804	6589	99	17.289
GMSK	32	4813	805	9168	163	14.55
GMSK	64	6892	808	13071	32	10.336

The operating frequency of design in FPGA depends on the architecture of the algorithm. The precision bitwidth for the implementation is considered as 12 bit for floating point and 12 bit for integer representation. The performance evaluation of algorithm is carried out by two parameters namely α -probability of miss-detection and β -probability of false detection and are computed as

$$\alpha = 1 - E_A[\hat{\phi} \,|\, "on"] \quad (8)$$

$$\beta = P(\hat{\phi} = 1 \,|\, "off") \quad (9)$$

where, E_A (.) is the expectation value over Probability distribution function.

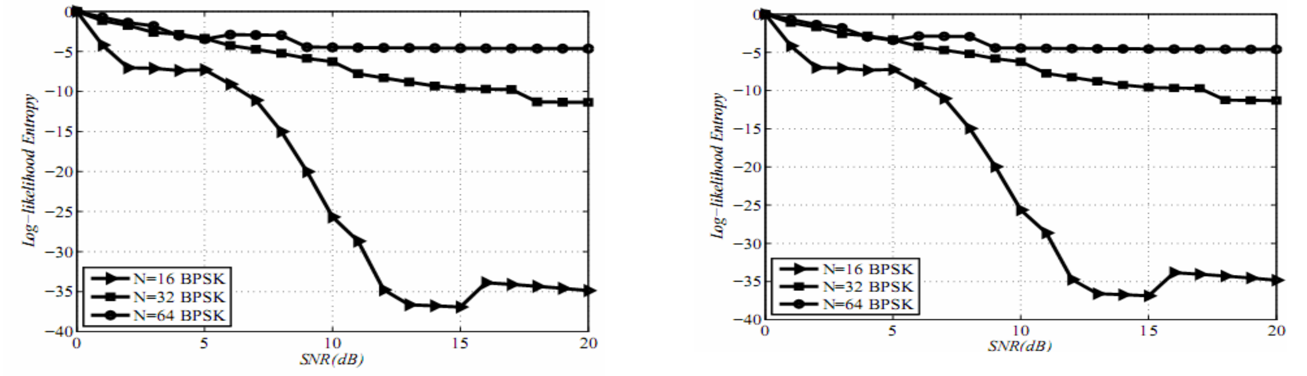

Figure 3 Log-likelihood entropy of BPSK signal using MATLAB and FPGA

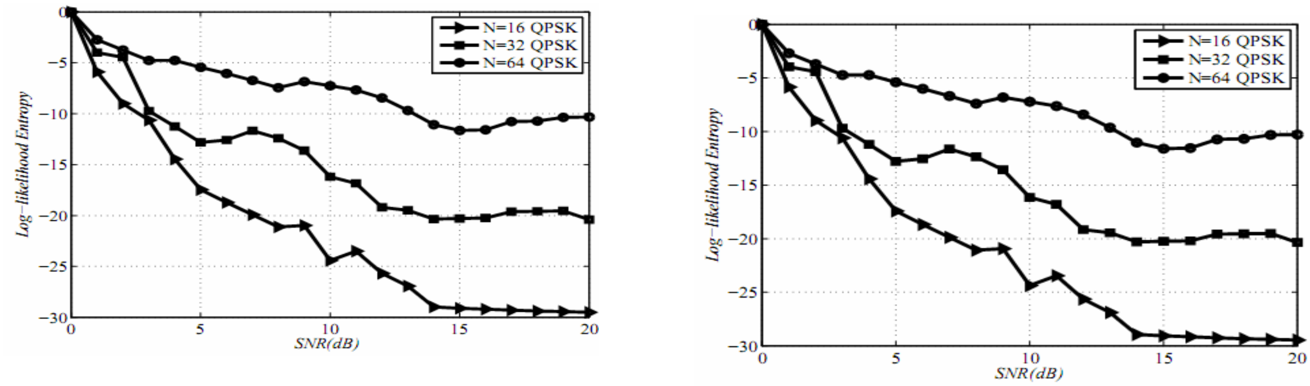

Figure 4.Log-likelihood entropy of QPSK signal using MATLAB and FPGA

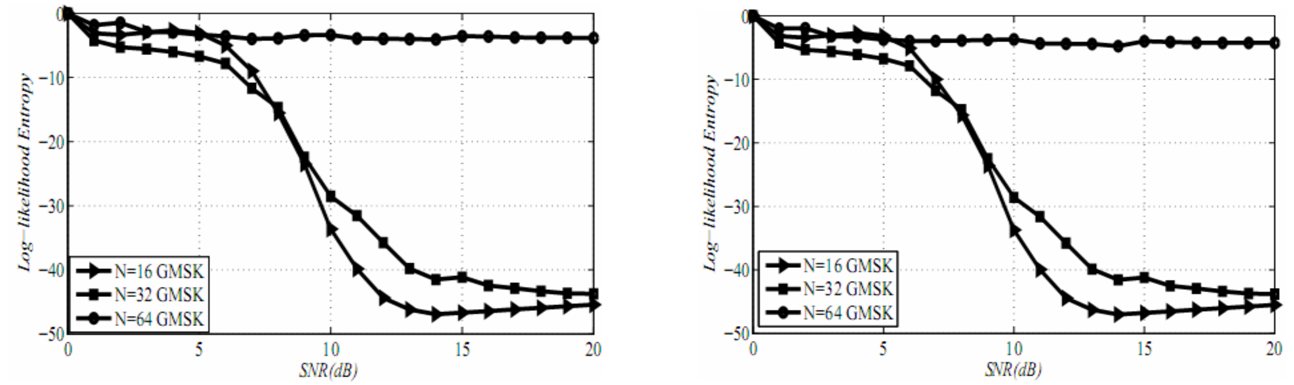

Figure 5.Log-likelihood entropy of GMSK signal using MATLAB and FPGA

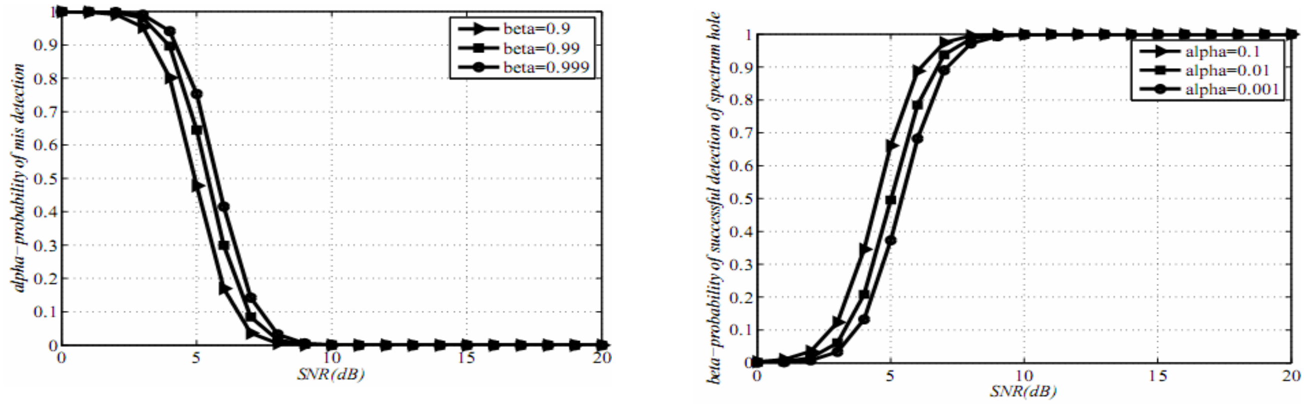

Figure 6.The SNR α/β dependencies of BPSK signal for N=16

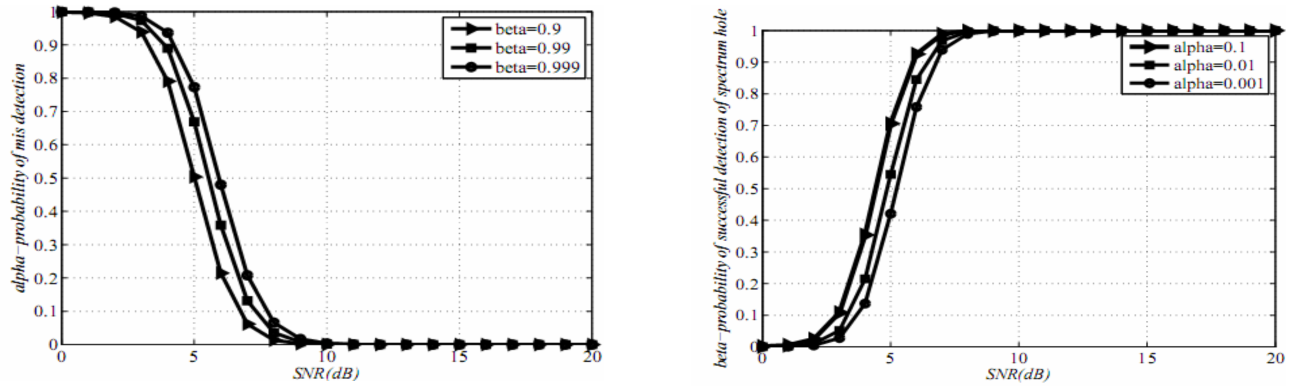

Figure 7.The SNR α/β dependencies of QPSK signal for N=16

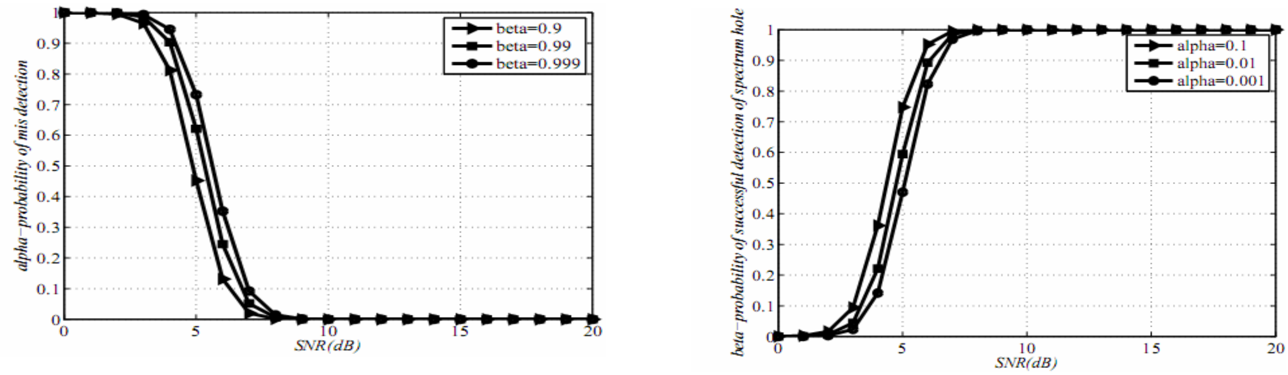

Figure 8.The SNR α/β dependencies of GMSK signal for N=16

Table II
COMPARISON OF RMSE FOR BPSK, QPSK AND GMSK SIGNALS

Modulation	No of samples (N)	RMSE for Entropy	RMSE for log- likelihood entropy
BPSK	$N = 16$	0.03	0.429
BPSK	$N = 32$	0.03	0.429
BPSK	$N = 64$	0.03	0.429
QPSK	$N = 16$	0.031	0.432
QPSK	$N = 32$	0.031	0.432
QPSK	$N = 64$	0.031	0.432
GMSK	$N = 16$	0.0454	0.09891
GMSK	$N = 32$	0.0977	0.06472
GMSK	$N = 64$	0.0544	0.4315

Figure(6-8) depicts the detector performance for BPSK, QPSK and GMSK input signal with respect to different α and β values for the selected range of SNR. It is observed that the algorithm for detection of primary user signal gives good performance, for all BPSK, QPSK and GMSK signal with SNR greater than 0 dB. For validating this technique 40 test case signals of different modulation schemes with varying SNR are generated as shown in Table III. In this table, first, second and third coloumns represent channel number, channel bandwidth and type of signal respectively. VACANT in this column indicates absence of primary user signal and presence of random noise.

Column four indicates the SNR corresponds to the signal. Fifth column represents decision made by the detector. "1" represents presence of signal and "0" represents absence of signal. The results show that the algorithm is able to detect the presence of signal when SNR is equal to or more than 0dB without depending on considered modulation types.

CONCLUSIONS

In this paper, we have implemented the entropy based spectrum sensing technique for reliable detection of primary user activity in cognitive radio networks. Hardware/software co-simulation result for BPSK, QPSK and GMSK signal shows the successful implementation of the algorithm in FPGA for different

Table III
TEST CASE RESULT

Ch. No.	BW (MHZ)	Mod. Type	SNR (dB)	Decision
1	890.0-890.2	BPSK	3	1
2	890.3-890.5	QPSK	4	1
3	890.6-890.8	QPSK	2	1
4	890.9-891.1	GMSK	1	1
5	891.2-891.4	BPSK	6	1
6	891.5-891.7	VACANT	-1	0
7	891.8-892.0	GMSK	0	1
8	892.1-892.3	GMSK	-3	0
9	892.4-892.6	BPSK	-2	0
10	892.7-892.9	VACANT	-16	0
11	893.0-893.2	QPSK	1	1
12	893.3-893.5	BPSK	1	1
13	893.6-893.8	BPSK	5	1
14	893.9-894.1	GMSK	2	1
15	894.2-894.4	VACANT	-17	0
16	894.5-894.7	VACANT	-14	0
17	894.8-895.0	GMSK	5	1
18	895.1-895.3	BPSK	0	1
19	895.4-895.6	QPSK	-2	0
20	895.7-895.9	BPSK	7	1
21	896.0-896.2	GMSK	3	1
22	896.3-896.5	QPSK	0	1
23	896.6-896.8	BPSK	-1	1
24	896.9-897.1	QPSK	6	1
25	897.2-897.4	VACANT	-18	0
26	897.5-897.7	QPSK	-1	1
27	897.8-898.0	BPSK	-3	0
28	898.1-898.3	BPSK	3	1
29	898.4-898.6	VACANT	-13	0
30	898.7-898.9	GMSK	6	1
31	899.0-899.2	QPSK	3	1
32	899.3-899.5	BPSK	10	1
33	899.6-899.8	QPSK	3	0
34	899.9-900.1	GMSK	-1	0
35	900.2-900.4	VACANT	-12	0
36	900.5-900.7	QPSK	7	1
37	900.8-901.0	QPSK	1	1
38	901.1-901.3	VACANT	-2	0
39	901.4-901.6	QPSK	5	1
40	901.7-902.9	BPSK	4	1

sample size and SNR of input signal. This approach can be used for on-line spectrum sensing in real time environment. The proposed architecture for FPGA implementation works consistently with MATLAB simulation result. The operating frequency of design is approximately 15.5 MHz for BPSK, 15.2 MHz for QPSK and 17.2 MHz for GMSK signals of sample size 16. As sample size increases to 64, the operating frequency reduces to approximately 9.9 MHz . Further improvement in the algorithm for multi node spectrum sensing and corresponding architecture is under development to increase the efficiency and operating frequency of the design.

ACKNOWLEDGMENTS

The authors are thankful to the Department of Science and Technology, Government of India for providing necessary support to carry out this research work.

REFERENCES

[1] M. McHenry, “Frequency Agile Spectrum Access Technologies,” Federal Communications Commission, Swiss Federal Institute of Technology (ETH), Zurich, Tech. Rep. 703-761-2818, 2003.

[2] E. Zitzler, M. Laumanns, and L. Thiele, “Federal Communications Commission Spectrum Policy Task Force Report,” Federal Communications Commission, Washington, DC 20554, Tech. Rep. ET Docket No. 02-135, 2002.

[3] J. Mitola, “Cognitive radio: an integrated agent architecture for software defined radio,” Ph.D. dissertation, Royal Institute of Technology, Sweden, 2000.

[4] I. F. Akyildiz, V. M. C. Lee, Won-Yeol, and S. Mohanty, “Next Generation Dynamic Spectrum Access Cognitive Radio Wireless Networks : A Survey, Computer Networks:,” *The International Journal of Computer and Telecommunications Networking*, vol. 50, no. 13, pp. 2127–2159, 2006.

[5] H. Tang, “Some Physical Layer Issues of Wide-Band Cognitive Radio Systems,” in *Proceedings of IEEE Int’l Symp . Dynamic Specturm Access Networks , (DySPAN’05)*, Baltimore, MD, USA,, NOV 2005, pp. 151–159.

[6] B. Wild and K. Ramchandran, “Detecting Primary Receivers for Cognitive Radio Applications,” in *Proceedings of ACM Symp on Applied Computing 2002, SAC 2002*, Piscataway, NJ, NOV 2005, pp. 124–130.

[7] N. Han, S. Shon, J. Chung, and J. Kim, “Spectral Correlation Based Signal Detection Method for Spectrum Sensing in ieee 802.22 wran Systems,” in *Proceedings of the IEEE ICACT*, Graduate School of IT and Telecommunications INHA University,Incheon, Korea,Feb 2006, pp. 1765–1770.

[8] V. Nagaraj, Santosh, “Entropy Based Spectrum Sensing in Cognitive Radio,” *Signal Processing*, vol. no. 2, pp. 174–180, 2009.