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Efficient Memory Mapping in GSM Phones

Gurvinder Singh[1], Sheetal Bawane[2], Sumant Katiyal[3]
[1]. Malwa Institute of Technology,
gurvinderengg@yahoo.com
[2]. Malwa Institute of Technology
[3]. School of Electronics, DAVV, Indore

Abstract-**With the advancement in the technology that too wireless technology usage of cell phones is becoming significant. A cell phone have become versatile and portable electronics equipment rather then only used for receiving and making calls with the in creased uses of cell phone the memory requirement of cell phone are also increased many folds .the are the mobile with the capacity of 8 to 20 gb but still have limited storage for contacts and sms still contacts and ms cannot be stored directly in main memory. We propose a model in which all the 3 memories in mobile including mobile main memory, flash card memory and SIM memory can be efficiently utilized. All of them work in coordination with each other. In present the contacts can only be stored in mobile main memory or in memory. In our model contacts and sms, including emails and mms can be stored in flash memory card. This further neglects the use of SIM card reader and data cable. This technique is used first time in the any GSM and CDMA technique.**

***Index Terms*— SRAM**, SDRAM

I.INTRODUCTION

Our main goal is to achieve maximum utilization of mobile memory which includes mobile main memory, flash memory cards, and SIM memory. Our aim is to save contacts .SMS, MMS..etc direct in flash memory so that there could be no restriction on the quantity of contacts, sms, mms to be stored in a cell phone. For this purpose we proposes a navel memory mapping concept in mobile, which includes SD RAM, DDR2, SFFHDD, NOR flash, SRAM, PS RAM, NAND, NOR, all of those are navel standards which are used in mobile. New generation mobile devices are blazing trails in the 90 and 65 nanometer processes with unprecedented integration of IP blocks. Development risk and time to- market pressures make design-from scratch totally out of the question. Off the shelf IP blocks are redesigned help developers meet these system goals, and provide the necessary configurability to achieve optimal performance and power targets for product differentiation. New mobile products are now required to process massive amounts of data, which is driving significant change in the memory and storage architectures for these devices. Rapidly changing interface standards for mass storage devices, such a DDR2- SDRAM, NAND, NOR, and SFFHDD's, combined with the need to serve multiple elements of the SoC with varying degrees of performance, makes an ideal case for a sophisticated IP solution for memory and storage control.

Mobile Memories

A. SRAM

Static random access memory (SRAM) is a type of semiconductor memory where the word static indicates that, unlike dynamic RAM (DRAM), it does not need to be periodically refreshed, as SRAM uses bistable latching circuitry to store powered.

B. DRAM

Dynamic RAM (DRAM) is the type of memory chip used for most of the main memory in a modern PC. DRAM is widely used due to its high density i.e. large number of bits can be stored in a single chip. DRAM chip have tiny capacitors in the chip as that memory cells that retain a charge to indicate a bit. It's limitation lies in the fact that it needs to be refreshed constantly; as the electrical charges in the individual memory capacitors will drain and the data will be lost. Refreshing is generally done whenever the system memory controller takes a tiny break and accesses all the rows of data in the memory chips.

C. RAM (PSRAM) or CELLULAR RAM

PSRAM or PSDRAM is dynamic RAM with built-in refresh and address-control circuitry to make it behave similarly to static RAM (SRAM).

It combines the high density of DRAM with the ease of use of true SRAM. PSRAM (made by Numonyx) is used in the Apple iPhone and other embedded systems. Some DRAM components have a "self-refresh mode".

D. SDRAM

SDRAM refers to synchronous dynamic random access memory, It is DRAM dynamic random access memory with a synchronous interface. Conventional dynamic random access memory (DRAM) usually have an asynchronous interface that certainly means that means that it responds as quickly as possible to changes in control inputs. SDRAM has a synchronous interface, which certainly means that it waits for a clock signal before responding to control inputs and is to be always synchronized with the computer's system bus.

E. MOBILE SDRAM

Synchronous Dynamic Random Access Memory (SDRAM) is the most commonly used memory today. It popularity lies in the fact that it provides high-density storage solution that too at a low cost. Conventional SDRAM is not the best option while designing handheld and portable devices (such as personal digital assistants (PDAs), portable smart devices, portable medical devices, digital cameras and portable media players). In the aforesaid applications due priority is given to the low power consumption. Whereas Conventional SDRAMs are not power-sensitive devices so choosing mobile SDRAMs is one of the best solutions. Mobile SDRAMs essentially the low power versions of conventional SDRAMs. Mobile SDRAMs provide the memory density required for complex handheld and portable applications, and at the same time, extend battery life and reduce cost. Core voltage of the Mobile SDRAMs is lower than that of the conventional SDRAMs. These manufactured using advanced process technology.

F. Cell (Microprocessor)

Cell is microprocessor architecture jointly developed by Sony Computer Entertainment, Toshiba, and IBM, an alliance known as "STI". The architectural design and first implementation were carried out at the STI Design Center in Austin, Texas over a four-year period beginning March 2001 on a budget reported by IBM as approaching US$400 million. Cell is shorthand for Cell Broadband Engine Architecture, commonly abbreviated CBEA in full or Cell BE in part. Cell combines a general-purpose Power Architecture core of modest performance with streamlined co processing elements which greatly accelerate multimedia and vector processing applications, as well as many other forms of dedicated computation

G. Flash memory

It is a non-volatile form of computer memory and it can be electrically erased and reprogrammed. This technology is primarily used in memory cards and USB flash drives for general storage and transfer of data between computers and other digital products

RELATED WORK

In [1] as the size of reconfigurable fabrics increases we can envision entire applications being mapped to a reconfigurable device; not just the code, but also the memory. These larger circuits, unfortunately, will suffer from the problem of a growing memory bottleneck. In this paper we explore how mobile memory techniques, inspired by cache-only memory architectures, can be applied to help solve this problem. The basic idea is to move the memory to the location of the access. Using both an analytical model and simulation several different memory movement algorithms were investigated

II MODEL

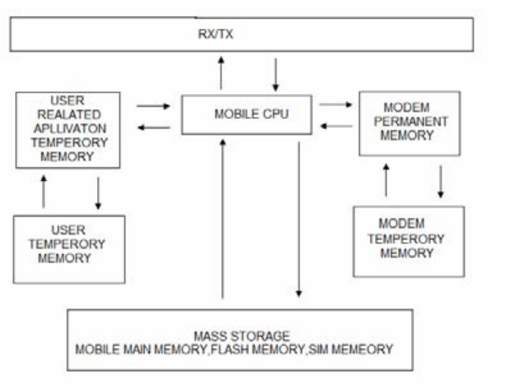

Figure1 Mobile memory interfacing

In above figure the mobile CPU unit makes an interface with each section of memory. And it works in coordination with all the sections of memory. The instruction set for internet related application is stored in modem permanent memory which can be SRAM, PSRAM etc. And the temporary memory for the modem is also been separated form mass storage when the down loading is done it is done to mass storage but temporary settings are stored in temporary memory. User related application is stored in permanent memory for user related application and other in temporary memory. When the sms comes to our cell it is interpreted by CPU and directly stored in mass memory using the instructions set present in user related application memory. And same can be done with the contacts as the CPU makes the direct connection whit flash memory then it is easy to store SMS, MMS, contacts in flash memory as well. When any of the call comes to our cell then the scanning of the contact folder which can be in any of the three memories can be easily done. And at the time of making the call as well the process can be fast enough. Rest how exactly the model works is been given in flow chart.

Flowchart

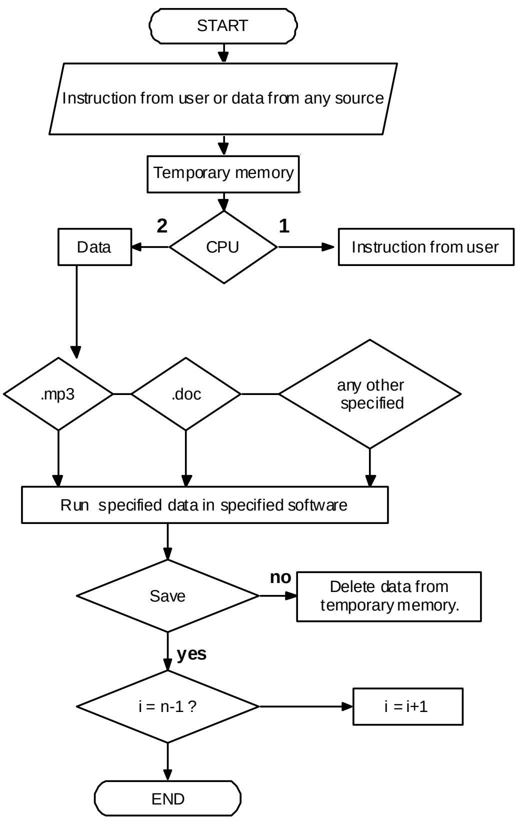

Figure2 Flowchart 1

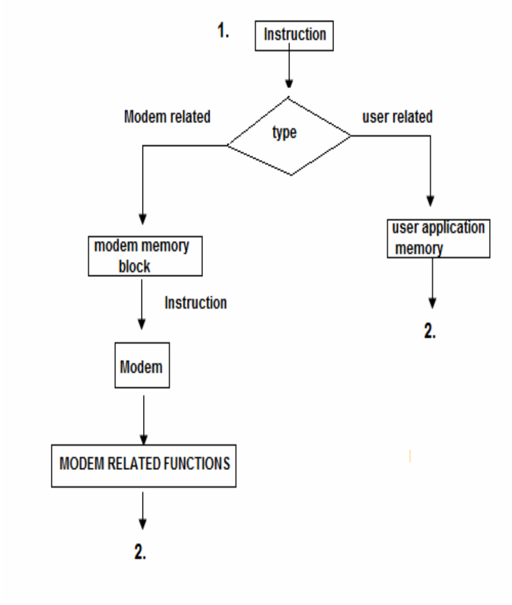

Figure 3 Flowchart 2

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